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AEROSPACE SENSOR COMPONENT AND SUBSYSTEM INVESTIGATION AND INNOVATION-2 COMPONENT EXPLORATION AND DEVELOPMENT (ASCSII-2 CED)

Delivery Order 0002: Volume 1 – Reconfigurable Aperture Antenna Virtual Prototyping (RFIC Radar-on-a Chip Component Design And Re-Use Development)

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14. ABSTRACT

The main task item that was common to all the tasks in the statement of work was the capture of new methodologies in RF and analog design flows. RF/Analog design flow methodologies can be difficult to sustain for defense electronics programs. The enabling outcome of the circuit synthesis development was an improved capability in developing RF/Analog design flows in defense design centers. The extension of the synthesis methods to larger circuits involving both analog and digital modules will enable the achievement of higher performance systems using new architectures. These architectures, that allow the RF and analog modules to be reconfigured, will allow designers to develop systems such as Software Radars and Software Electronic Warfare Receivers.

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Executive Summary

This Executive Summary provides an overview of the research program performed on delivery order two of the ASCSII-2 contract #F33615-00-D-1726-0002. The Introduction gives the context of the Statement of Work, followed by the Research Work section, which describes the content in three main tasks: (1) LNA Design Flow, (2) Re-use and Analog Firm, and (3) Design Center and CAD tools. The remaining sections, Main Results and Conclusions, include the key outcomes and recommendations.

Introduction

This document reports the research program performed by Prof. Steven Bibyk and several of his students from The Ohio State University (OSU) for the Air Force Research Labs (AFRL) design center led by Dr. Gregory Creech of the Sensors Directorate at Wright-Patterson Air Force Base. Systran Federal Corp. managed the research program.

The research program evolved from a National Research Council Summer Faculty Fellowship program by Prof. Bibyk at the AFRL design center and the increased effort by the Dept. of Defense to fund research for RF and Analog Integrated Circuit Synthesis, such as the DARPA NeoCAD program.

The main task item that was common to all the tasks in the statement of work was the capture of new methodologies in RF and analog design flows. RF/Analog design flow methodologies can be difficult to sustain for defense electronics programs. The enabling outcome of the circuit synthesis development was an improved capability in developing RF/Analog design flows in defense design centers. The extension of the synthesis methods to larger circuits involving both analog and digital modules will enable the achievement of higher performance systems using new architectures.

These architectures, that allow the RF and analog modules to be reconfigured by the digital processing cores, will allow designers to develop systems such as Software Radars and Software

Electronic Warfare Receivers, similar to the objective of developing Software Radios, the latter being developed for both commercial and military applications.

The Ohio State University students who participated in this research were David Bayer, Jason Parry, John Fisher, Edward Murphy, and Jason Abele. David Bayer completed his M.S. thesis, titled: “Methodology for Reuse of High Speed Mixed Signal and RF Integrated Circuits.” John Fisher is completing his PhD and is now working for a company that spun out of MIT Lincoln Labs via his experience in this research program. The other students are completing their MS theses, and all thesis documents will be made available to the AFRL design center.

Research Work

This section integrates the research work of three main tasks: (1) LNA Design Flow, (2) Re-use and Analog Firm, and (3) Design Center and CAD tools.

LNA Design Flow

This section of the report describes the LNA design work and demonstrates the type of content which needs to be considered for design reuse in the next section. Low Noise Amplifiers (LNA) were designed and fabricated in two versions of the MITLL Silicon on Insulator (SOI) process. These two versions of the process were referred to as MP5 and MP6. Test results on the MP5 run indicated a design error that was corrected on the MP6 run. Test results were not performed on the MP6 devices. The main outcome of the LNA design work was to have a design database of all content needed for IP design-reuse, which is described in the next section. The LNA design work also demonstrated the sensitivity of circuit behavior to the layout decisions. Thus, jointly simulating electro-magnetic (EM) effects and circuit effects are necessary, and the EM effects can only be simulated from the layout geometry. The sensitivity to EM effects at the size of IC geometries is somewhat surprising, since the IC geometries were tens to hundreds of times smaller than the wavelengths of interest. In these regimes, transmission line and other EM effects are often negligible. However, the conductivities of wiring layers on an IC show much greater loss attenuation than that of discrete RF designs. Thus, even wire length geometry much smaller than a wavelength will attenuate and change S parameters design values. Due to the layout sensitivity, the synthesis of RF designs must include EM calculations, which made the design

flow more difficult to automate. In many cases, both at OSU and in the AFRL design center, many of the design decisions were determined by the designers as opposed to the synthesis tools.

RF/Analog Re-use and Analog Firm

This section of the report describes the work done for a design re-use design flow for RF/Analog and Mixed Signal. The work involved working with members of the Virtual Socket Interface Alliance (VSIA), an industry organization to facilitate the use of Integrated Circuit (IC) Intellectual Property (IP). VSIA facilitates the use of IP by developing standards for delivery of IC IP. These standards are embodied in documents and manuals, the main ones referred to as Extension Specifications. Extensions are needed since the delivery of IP often amounts to adding specifications to the original specification of the IC module being exchanged between the IP provider (seller) and the IP integrator (customer).

AFRL Design Center and NeoCAD tools

This section of the report summarizes the work done by Steve Bibyk and his students at the AFRL design center and at the various NeoCAD related meetings and review sessions. A number of design documents were developed and exchanged with the AFRL design center and NeoCAD community. There is also a review of exercising some of the NeoCAD tools, such as the Freeda simulation environment.

Main Results

The key result from RF/Analog synthesis research is that the most effective strategy is to accelerate what an experienced designer needs to get done. Accelerating the activities of an experienced designer also turns out to be the main requirement for design re-use and RF/Analog IP. In simplistic terms, an experienced designer runs many different types of simulations to make design decisions at the schematic level. A simple term for these decisions is sizing. Once all the sizing decisions are done, IC layout is the next step. IC layout is tedious, time consuming, and needs major rework if any schematic sizing decisions need to change. Speeding up IC layout is also a key requirement for synthesis and re-use. One way that a method helps layout is to reduce the time needed for other task, such as having to resize schematics. Another effective method to speed up IC layout is to use parameterized cells (p-cells) in a place and route tool. The

combination of p-cells with place and route will be referred to as layout generators. Finally, after layout is accomplished, the schematics need to be updated to include the layout parasitics. The Neolinear tools were one of the most effective CAD packages to encompass the above acceleration of the RF/Analog design flow.

Unfortunately, there is no standard language or set of constructs to describe the above acceleration methods. One would hope that since simulations are model driven approaches, that standard modeling languages such as HDL-AMS (Hardware Description Language-Analog and Mixed Signal) would be used. However, this is not the case, since HDL-AMS does not standardize the simulation method, only the modeling method. Nevertheless, since HDLs are inherent in nearly all recent innovations in digital and software design flows, and many mixed signal systems, such as Software Radar, will use large digital cores and software to achieve new performance, HDL-AMS will eventually need to be fixed for RF/Analog re-use and synthesis.

The Analog Firm group in the VSIA worked on the development to standardize the methods for RF/Analog IP. Two of the main methods were to use the MUSE language from Barcelona-Design, which was being released for public use. The other method was to use the HDL-AMS development from Mentor Graphics, since HDL-AMS was also an IEEE standard. Unfortunately, both methods ran into roadblocks. Barcelona Design has folded as a company and the MUSE language is no longer available. The HDL-AMS approach at Mentor Graphics is not being positioned for RF/Analog synthesis at this time. At present, the only remaining language and set of constructs for RF/Analog re-use are the proprietary constructs that are part of the Neolinear CAD tools.

There are several concerns when relying on proprietary constructs for re-use. First, in many design groups, designers use tools from a variety of CAD vendors. In many cases, a specific task is accomplished in a point tool, and in general, the complete set of tools from a given vendor is not the best set of point tools. For example, the behavioral modeling of RF modules in ADS is more effective for the designer than using Verilog-AMS for RF modules in Cadence, since the ADS tool has an efficient method to curve fit to determine the behavioral module parameters. RF testbenches are often more effective in ADS than in Cadence SpectreRF.

RF/Analog IP re-use seems to have a more viable path when done within the same organization. In this case, the loss of intellectual property by the provider may not have the same level of concern. The final task of the research program was to provide some methods and software for internal re-use. The software would be used to automate the production of design capability content, by capturing in one sheet the key demonstration of a working IC module. The sheets would contain object views of design content such as schematics, simulation plots, layouts, and descriptions of the object views. A UNIX/latex script file would organize the sheets into presentation format for designers that are IC integrators.

Conclusions and Recommendations

Several LNA modules were designed to completion and fabricated to obtain insight into all the constructs needed for RF/Analog re-use. Although there were testing difficulties with the LNAs, the design activity did discover many of the activities and design content needed for an LNA design module. Another reason for performing the LNA design was to do the initial design work for reconfigurable RF modules. Future system designs such as Software Radars are expected to have RF modules that are reconfigured by the digital processing core for higher performance. For example, our LNA was fabricated in the MIT LL SOI process, which was part of a radar system design that used proprietary digital signal processing to enhance dynamic range, such as nonlinear compensation for enhancing Spurious Free Dynamic Range (SFDR). Nevertheless, the requirements for the RF and digital processing modules were such that the modules could be designed separate from each other and brought together at the final integration step. However, a method to achieve additional dynamic range would be to make the LNA adaptable, such that its operation depended on the strength of the received radar signal. For very weak signals, the LNA could be adapted to improve noise figure, whereas for stronger signals, the LNA could be adapted for improved linearity. The adaptation would be controlled by the digital core to enable signal processing to determine the adaptation process.

The main benefit of doing the LNA was to understand all aspects of the RF design process for re-use related synthesis. Bayer's Chp. 2 on Design Re-use methodologies (thesis title also) conveys useful content. Verilog A didn't work well for re-use, it is better in ADS. The RFDE software enabled Neolinear to do RF synthesis.

Barcelona Design disappeared. Mar and Navraj left and Singh moved on. The hypothesis was that Analog and RF reuse could be specified independent of CAD tools, and so could synthesis, which is the new element to analog IP. However, at this time, analog synthesis, and its utilization for analog IP, is CAD vendor specific, with the Cadence tools being the leading vendor for the AFRL design center.

In RF/Analog design flow, much of the design content is captured in the CAD tools database. The design content is not evident in the design documentation. In many cases, multiple CAD tools need to be integrated together, for example, Cadence, ADS, digital tools in either Synopsis or Mentor Graphics, and Microwave Office. Since each CAD tool uses a different database and scripting methodology, there are problems in using the tools. Much of a design is specific to a CAD tool vendor.

System development will still need to use some combination of HDLs and behavioral macromodeling. Macromodeling in Cadence was inefficient. Not only do circuits need to be macromodelled, but so do performance calculations. This is known as Results extraction from the simulation waveforms. In cadence, this is often accomplished using the calculator function after running a simulation. Another possibility is to use the ocean scripting language. ADS built in these types of operations so that they can be placed on a schematic for a simulation and thus be part of an optimization routine for synthesis.

I. Introduction

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The main task item that was common to all the tasks in the statement of work was the capture of new methodologies in RF and analog design flows. RF/Analog design flow methodologies can be difficult to sustain for defense electronics programs. This observation drove the DARPA NeoCAD program to innovate new design methodologies, based on accelerating the design flow by supporting the development of RF/Analog synthesis software. The enabling outcome of the circuit synthesis development was an improved capability in developing RF/Analog design flows in defense design centers.

The further development of RF/Analog synthesis will enable not only better design flows, but also improve the re-targeting of working designs to new and higher performance fabrication technologies. In addition, the extension of the synthesis methods to larger circuits involving both analog and digital modules will enable the achievement of higher performance systems using new architectures, similar to those described in this report.

These architectures, that allow the RF and analog modules to be reconfigured by the digital processing cores, will allow designers to develop systems such as Software Radars and Software Electronic Warfare Receivers, similar to the objective of developing Software Radios, the latter being developed for both commercial and military applications.

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II. Research Work

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A. LNA Design Flow

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After the MP5 LNA designs were completed and scheduled for fabrication, we submitted an initial test plan to the AFRL mixed signal design center on the LNA designs that are being fabricated in the MITLL Silicon on Insulator MP5 process. The LNA designs used the inductor cells that were designed by Kevin Idstein and Prof. Rojas.

We submitted Final Report items for MP5 testing results to Scott Axtell. The key conclusions are summarized next.

Initial testing of the X band LNA showed no appreciable gain. The LNA passive tank circuits were designed to resonate at 9GHz, so the initial lack of gain was attributed to insufficient

transistor transconductance at 9GHz; unfortunately, since the tank circuits are not tunable, it does not appear possible to test the gain operation at lower frequencies that would exhibit transistor gain.

Another possible cause of gain degradation was the use of a 50 ohm resistor in parallel with the tank circuits. As described in the attached OSU LNA test plan PDF document, the 50 ohm resistor was initially used to improve the S22 matching criteria. However, later calculations showed that the 50 ohm matching resistor severally degraded gain.

An experiment was performed on the 2 stage LNA design to remove the 50 ohm resistor and to measure gain at X band frequencies, even with poor S22 matching. The 50 ohm resistor was successfully removed by sending a large enough current into the output pad so as to evaporate the resistor. A driving voltage of 8v was found to be sufficient to evaporate the resistor. Testing of the modified LNA still showed no appreciable gain.

Further evaluation of the LNA design showed that the output connection for the two stage LNA was on the supply side of the output inductor. Even though simulations predicted there would be gain on the supply side of the output inductor, this was found to be an artifact of the small signal simulation process and would not occur in a tested design.

The single stage LNA design did have its output connection on the non-supply side of the inductor. The single stage LNA also had a 50 ohm resistor for S22 matching that was degrading gain. However, efforts to evaporate the 50 ohm load resistor on the single stage LNA were unsuccessful. This was due to a change in the scattering parameter network analyzer to incorporate a new differential scattering parameter measurement system.

The problems found on the OSU LNA design on the MP5 run were corrected on the MP6 run. A different output matching stage was used that did not require the need of a 50 ohm resistor. Also, LNAs were designed for both S band and X band operation, to increase the likelihood of sufficient transistor gain at the desired center frequency.

This section describes the LNA designs performed for the MP6 run of the MITLL FDSOI technology. The designs were optimized using the Agilent ADS design tool and layouts were developed in the Cadence IC design tools. The design work was performed by Edward Murphy, Jason Parry, and Steven Bibyk at The Ohio State University.

The LNA design consisted of a single cascade stage of relatively small NMOS transistors. To keep the input gate noise low, a maximum width for each finger of the transistor width was chosen around 10 μm. By using multiple fingers to make up a single transistor, the overall input resistance and current density are improved at the expense of area and some capacitances. Minimum length gates are also chosen, which for this technology is 0.2 μm drawn. The final designed transistor dimensions were 20x12.75 μm x 0.2 μm for the S-Band LNA and 10x9 μm x 0.2 μm. Inductive source-degeneration was used as well as an inductor for the output-stage tank. This resulted in three transistors surrounding the cascade pair with fairly large capacitors for the output matching and another for a large DC-block connection to the output bondpad.

The S-Parameter measurements use cascade probes with G-S-G probe pads. The bondpads were designed for this technology to result in 50μm impedance to match the cascade probes. Based on the top metal width and reasonable areas to contact the probe pads, the pads were designed to be approximately 75 μm square with 35 μm space to the ground pads on either side.

The LNA design was straight-forward and resembles the schematic in regards to the placement of the passive and active devices. Three probe pads are to be used to test the LNA. Input, Output, and Vdd supply probe pads all share the same ground connection. Two designs were used to assess the difference in layout styles between microwave designers and traditional analog design. One uses a large ground plane to provide for good return paths and coplanar waveguides. Simulations were performed to estimate a 50 ohm transmission line and width and spaces to ground plane chosen accordingly. The second layout only uses a solid ground ring around the LNA to ensure a good ground connection.

The transistor layouts were designed for large enough metal and number of contacts for low resistance and high current capacity. The large numbers of fingers were joined together with a

common metal structure and minimal wiring. This metal is tapered and connected to the corresponding inductors with the corresponding inductor widths. The input inductor was designed to be 4 μm wide to reduce the overall size of the large inductor area. The two inductors used between Vdd and Gnd are chosen to be 10 μm wide to handle a large DC current which the cascoded pair are biased at.

The final consideration in the layout correspond to arbitrary distances and widths used for ground and supply nets. The ground plane was kept a reasonable distance away from the edges of inductors and capacitors to not affect their values or introduce coupling. The Vdd input bias on the gate of the second cascoded transistor is wired with a small line and only used for DC biasing. Finally, a decoupling capacitor is placed between the Vdd and ground nets with a large 1 pF MOS capacitor.

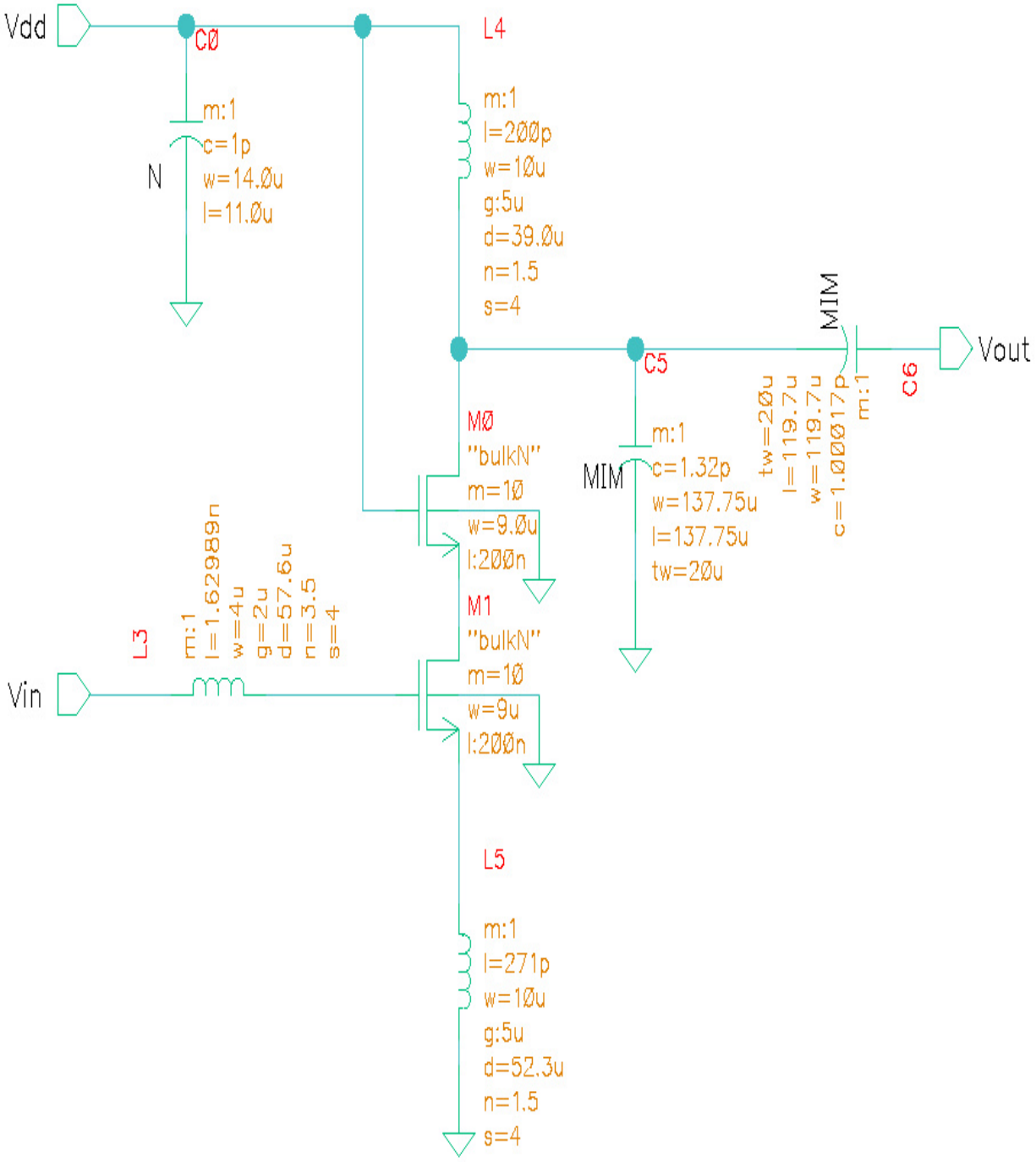
Twelve additional layouts were included for individual component test and characterization. A 2-port S-Parameter G-S-G test cage structure was designed to fit all devices to be tested. The use of a common structure allows accurate S-Parameter characterization and device testing at key frequencies when included with de-embedding structures. Four of the test layouts included were the open, short, through, and load structures needed for de-embedding. Six layouts were added inside the common test structure to isolate each circuit component. The isolated circuits consisted of two inductors to compare their S-Parameters against our simulations, with and without a shield underneath. A 1pF metal capacitor was placed in a test frame also. A MOS capacitor was designed for possible use as a varactor. Both types of transistors used were isolated for individual device characterization over the operating frequencies and I-V characteristics.

Two additional test layouts were included to be able to measure the overall S-Parameter performance of the entire input and output stages. One structure included the entire layout from the input of the LNA as seen from the input gate of the transistors. The second test structure included the entire output stage of the capacitors and inductor, which is driven by the output of the cascoded transistors. With this information and models for the transistors, it is hoped a more complete behavioral model simulation may be verified against hardware measurements.

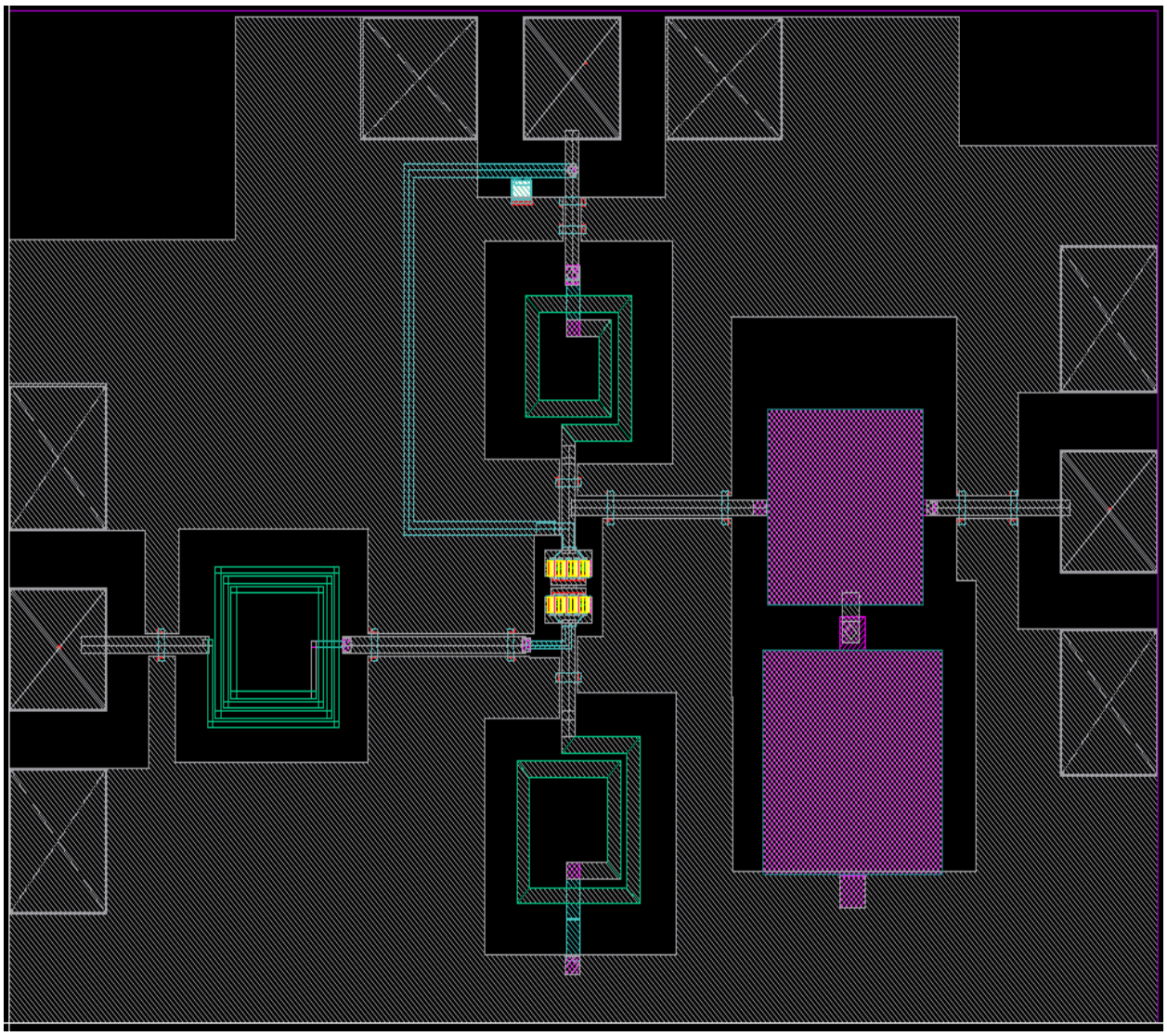
Research opportunities presented themselves toward the end of the MP6 LNA layout. One such topic was the characterization and design of passive devices in high frequency circuits. It is clear from discussions within our group and with our colleagues at AFRL that there are a number of open questions pertaining to the design of passives in a fully depleted Silicon-on-Insulator process. Another issue that needs further investigation is the role and engineering tradeoffs associated with the output matching network in the source inductor degenerated LNA topology. Specifically, we need to develop a design strategy for determining the inductor value at the drain node of the LNA's cascoded transistor and the corresponding capacitance value and configuration needed in the output matching network.

The following sections overview the design flow and design content for the MP6 designs.

X band LNA schematic in Cadence



X band Layout in Cadence



Test plan development for FDSOI MP6 designs

Ed Murphy wrote up a test plan for the OSU MP6 LNA designs at S band and X band.

In order to optimize RF receiver design, much attention must be given to the input stage. One key component of this stage is the low noise amplifier or LNA. By inspecting the equation for calculating the noise figure of a cascoded receiver system (1), we can see that the noise figure at the front of the receiver chain plays a substantial role in the overall system noise figure.

$$NF_{tot} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{Ga_1} + ... + \frac{NF_m - 1}{Ga_1 ... Ga_{(m-1)}} \quad (1)$$

NF_m = Noise Figure of stage m.

Ga_m = Gain of stage m.

This equation shows that by minimizing the NF and maximizing the Ga, the total NF will be reduced. Our goals then, for the design of the S-band and X-band LNA's will be as follows:

- NF – as low as possible.
- Gain – as high as possible.
- Zin – 50 Ω
- Zout – 50 Ω
- Reverse Isolation (S12) – as low as possible.
- Power Consumption – as low as possible.

Obviously, from these design goals some tradeoffs will need to be made. In particular, for gain to be high, the power consumption will rise. Also, as Gain increases, the noise figure increases. Yet, another design consideration will be the physical size of the components. These designs will be for the MITLL 0.18 μm Low Power FDSOI CMOS process.

Typically, LNA design begins with some basic hand calculations for key values that will be used to define an initial design space. Dr. Thomas H. Lee outlines this approach in "The Design of CMOS Radio-Frequency Integrated Circuits." The topology chosen for both LNA's will consist of cascoded transistors with inductive degeneration. The approach is as follows:

1) Determine the optimal transistor width (2).

$$W_{opt} \approx \frac{1}{3\omega L C_{ox} R_S} \quad (2)$$

2) Choose Drain current (I_D), such that you satisfy Power considerations.
3) Calculate Source inductance (L_S), with equations (3), (4), (5), and (6).

$$L_S = \frac{R_S}{\omega_T} \quad (3)$$

$$\omega_T = \frac{gm}{C_{gs}} \quad (4)$$

$$gm = \sqrt{2\mu nCox\frac{W}{L}I_D} \quad (5)$$

$$C_{gs} = C_{ov} + \frac{2}{3}[Cox * W(L - 2L_D) \quad (6)$$

4) Compute the Gate inductance (L_g), by using the values above and the input impedance equation (7). Since all values are known except L_g, we can solve for it.

$$Z_{in} = j\omega(L_S + L_g) + \frac{1}{j\omega C_{gs}} + (\frac{gm}{C_{gs}})L_S \quad (7)$$

The problem with this approach is that it requires that the Spice model parameters are known, or easily obtained. As models become more complex, these parameters are not always easy to extract. For this reason, I chose a different approach.

Agilent Technologies' Advanced Design System (ADS) has powerful optimization algorithms and simulation capabilities. By leaving some design parameters as variables and defining desired performance goals, you can configure ADS to synthesize the design parameters that allow you to meet the design goals, if possible. Essentially what occurs is that you set up the schematic for your given circuit. You then specify any known or required parameters. The rest of the parameters are then left as variables. By constraining their optimization ranges and configuring the appropriate simulations, ADS then iteratively plugs in parameter values, simulates the design, and compares the results with goals set. It then changes the parameter values, re-simulates, and once again compares the results with the specified goals. It then determines the parameter changes that would cause the results to better approach the design goals. This is done again and again until the goals are met, or they are determined to be unreachable. If this occurs, you must then reconsider your optimization constraints or topology.

ADS has a number of optimization algorithms to choose from, these are listed in table 1.

Table 1. Available ADS Optimizers

Optimizer	Description
Random	Random search method with least-squares error function.
Gradient	Gradient search method with least-squares error function.
Random Minimax	Random search method with minimax L1 error function.
Gradient Minimax	Gradient search method minimax L1 error function.
Quasi-Newton	Quasi-Newton search method with least-squares error function.
Least P th	Quasi-Newton search method with least P^{th} error function.
Minimax	Two-stage, Guass-Newton/Quasi-Newton method with minimax error function.
Random Max	Random search method with procedure to internally negate the error functions to get error function maximization (worst case analysis).
Hybrid	Combines the Random and Quasi-Newton method.
Discrete	Discrete optimization, provided there is at least one discrete-valued optimization parameter in the design.
Genetic	Direct search method using evolving parameter sets.
Sensitivity	Single-point or infinitesimal sensitivity analysis of a design variable.

The following is an excerpt from the ADS manual on optimization.

"The optimizers are differentiated by their search methods and error function formulations. The *search method* determines how the optimizer arrives at new parameter values, while the *error function* measures the difference between computed and desired responses. The smaller the value of the error function, the more closely the responses coincide. When optimizers execute their search method, they substitute new parameter values to effect a reduction in the error function value."

"Optimization with Random Search is typically used initially. Optimization with Gradient search is generally used in later stages of optimization. Discrete optimization only affects discrete-

valued variables. The genetic algorithm search is well suited to the discrete and mixed (continuous and discrete) problems."

In our experience, we've found that the combination of Hybrid and Gradient work well. Using the hybrid algorithm initially to narrow the design space and then running the gradient algorithm, typically allowed me to avoid the problem of local minima.

The S-band LNA has a center frequency of 3.2 GHz. The schematic in ADS for this LNA is shown in Figure 1.

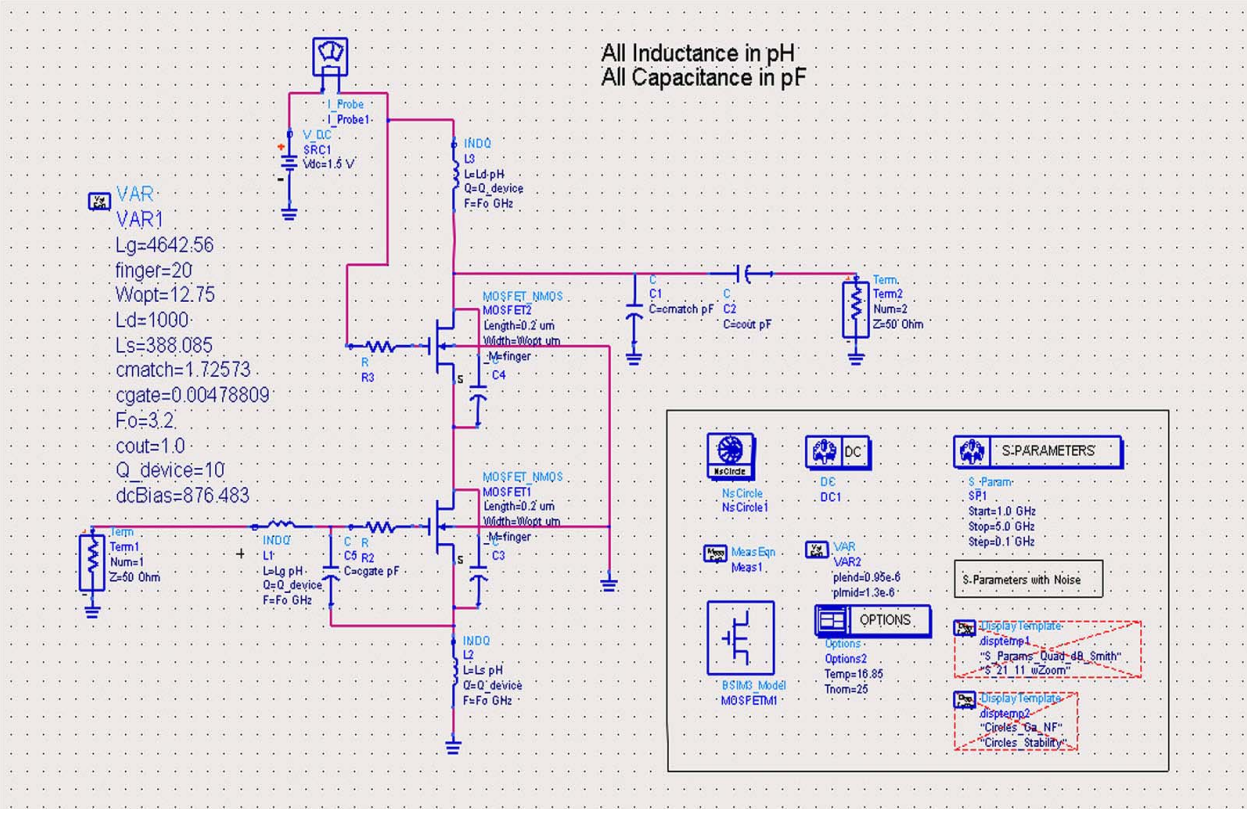


Figure 1. S-band LNA Schematic (ADS)

Here, you can see the overall setup for design simulation. Note that, of the parameters listed on the left, Q_device, cout, Fo, and fingers, are fixed; that is, they are not being considered for optimization. The Q_device parameter represents the Q of the inductors. This value was obtained from measurements on a previous run and is only an approximation. Cout was chosen to be 1pF to limit the area this device would use. Fo, is the design frequency (in GHz). Finally, the value

for fingers was chosen after it appeared that the transistor widths were going to be too large with only one finger. The rest of the parameters were determined via optimization. The I_probe component on the schematic is used to help determine the circuits' power consumption. The components in the box on the lower right are used to setup up simulations and define the transistor models.

Perhaps of more use in understanding the circuit itself is figure 2. This schematic is the same S-band LNA reproduced in Cadence. A disadvantage of using ADS is that its layout tools are designed for circuits at the PCB level. For this reason, we used Cadence for the actual layout. In order to perform LVS of our layout we re-created the schematic we used in ADS and inserted the optimized values where applicable.

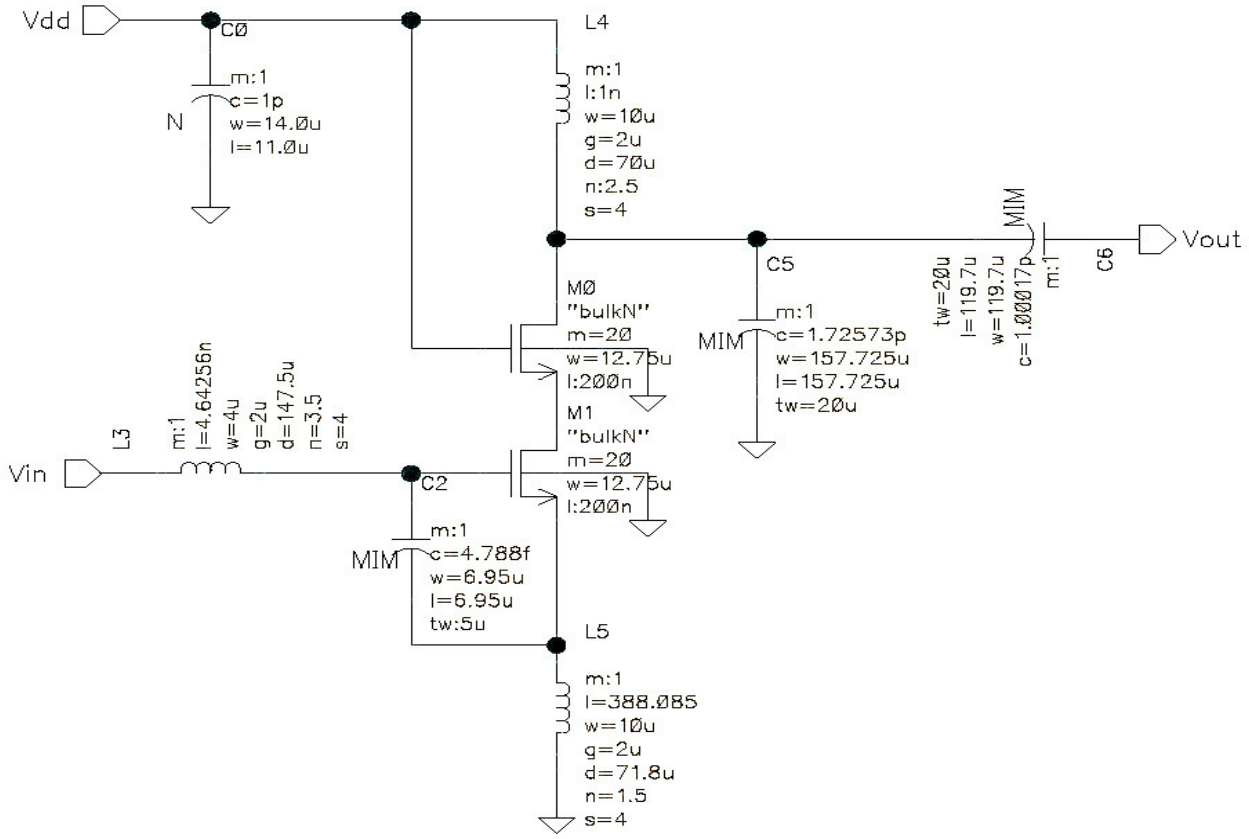


Figure 1. S-band LNA (Cadence)

Notice in this schematic that information regarding the devices' physical parameters is included. Where needed, some values were rounded to meet design rules. Of particular interest, is that while ADS gave us values for the capacitors and inductors, it could not tell us how these devices

would be realized. For the capacitors, we used the parameterized MIM cap cells provided with the design kit. For inductors, we used an average of the following three equations (8), (9), and (10) for square inductors.

$$L = 2.940531\text{E-}03\frac{n^2 davg}{1+2.75\rho}$$ Modified Wheeler Formula (8)

$$L = \frac{1.256637\text{E-}03 * n^2 davg * 1.27}{2}(\ln(2.07/\rho) + 0.18\rho + 0.13\rho^2)$$ Current Sheet Form (9)

$$L = 1.62E-03 * d_{out}^{-1.21} w^{-0.147} d_{avg}^{2.4} n^{1.78} s^{-0.03}$$ Monomial Expression (10)

Where:

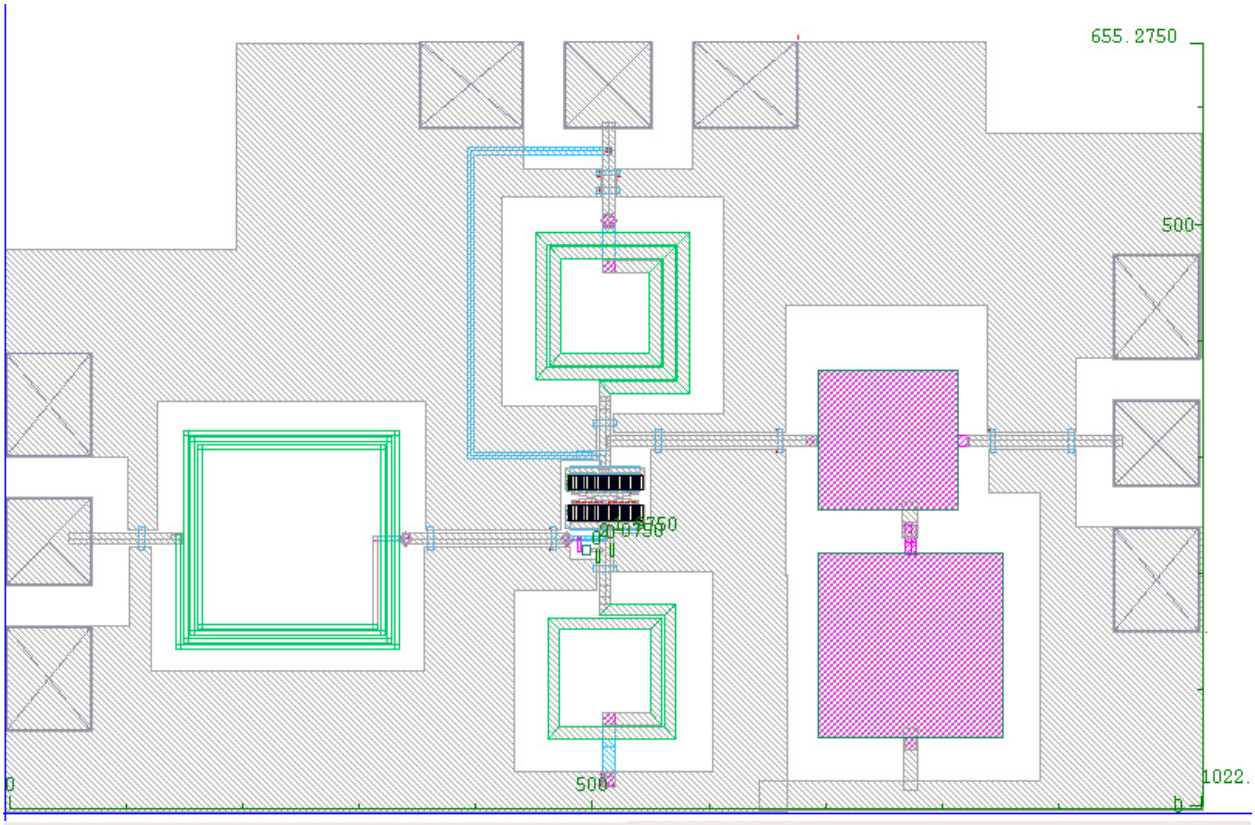
n = number of turns

$d_{avg} = (d_{out}+d_{in})/2$

$\rho = (d_{out}-d_{in})/(d_{out}+d_{in})$

s = space between spirals

The LNA layout from Cadence is also provided next.



GOAL

Goal
OptimGoal1
Expr="dB(S11)"
SimInstanceName="SP1"
Min=
Max=-30
Weight=7
RangeVar[1]="freq"
RangeMin[1]=3.1G
RangeMax[1]=3.3G

GOAL

Goal
OptimGoal2
Expr="dB(S22)"
SimInstanceName="SP1"
Min=
Max=-30
Weight=6
RangeVar[1]="freq"
RangeMin[1]=3.1G
RangeMax[1]=3.3G

GOAL

Goal
OptimGoal5
Expr="nf(2)"
SimInstanceName="SP1"
Min=
Max=.5
Weight=6
RangeVar[1]="freq"
RangeMin[1]=3.1G
RangeMax[1]=3.3G

GOAL

Goal
OptimGoal6
Expr="dB(S22)"
SimInstanceName="SP1"
Min=
Max=-20
Weight=2
RangeVar[1]="freq"
RangeMin[1]=2.9G
RangeMax[1]=3.5G

GOAL

Goal
OptimGoal4
Expr="dB(S21)"
SimInstanceName="SP1"
Min=20
Max=
Weight=6
RangeVar[1]="freq"
RangeMin[1]=3.1G
RangeMax[1]=3.3G

GOAL

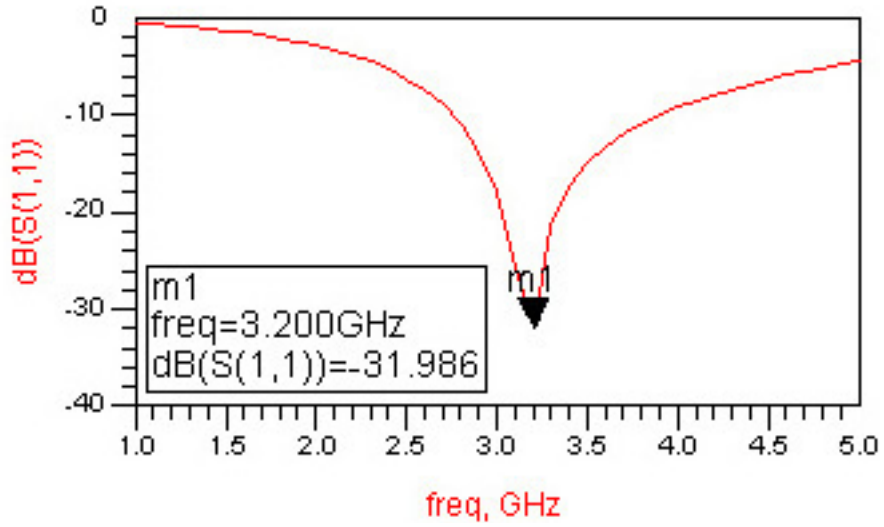
Goal
OptimGoal3
Expr="dB(S12)"
SimInstanceName="SP1"
Min=
Max=-30
Weight=2
RangeVar[1]="freq"
RangeMin[1]=3.1G
RangeMax[1]=3.3G

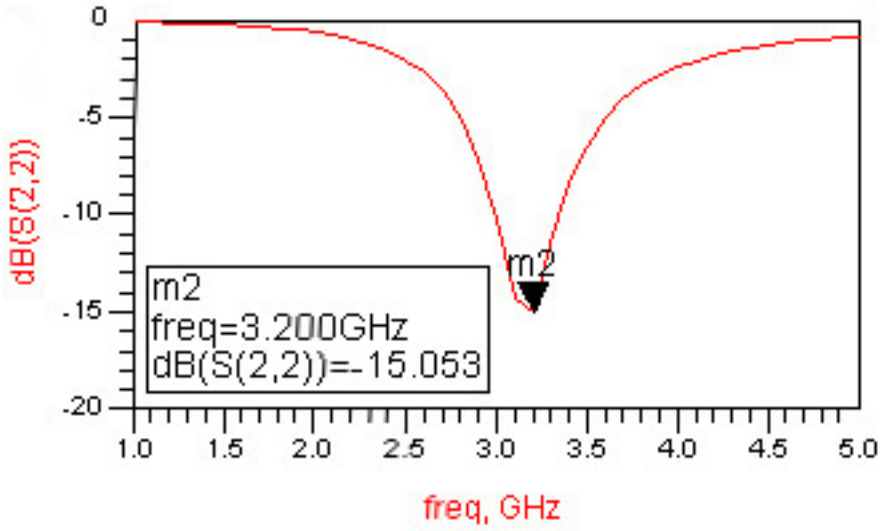
GOAL

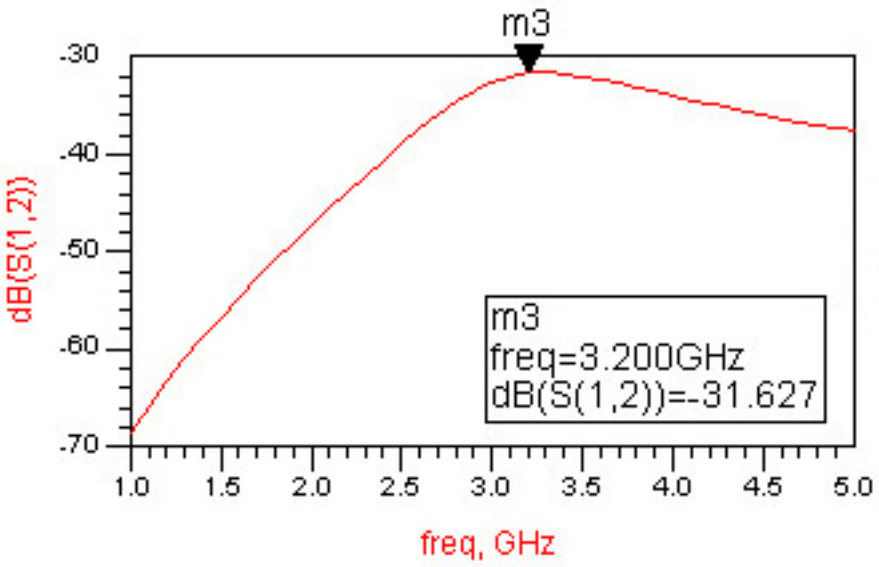
Goal
OptimGoal7
Expr="dB(S11)"
SimInstanceName="SP1"
Min=
Max=-20
Weight=1
RangeVar[1]="freq"
RangeMin[1]=2.9G
RangeMax[1]=3.5G

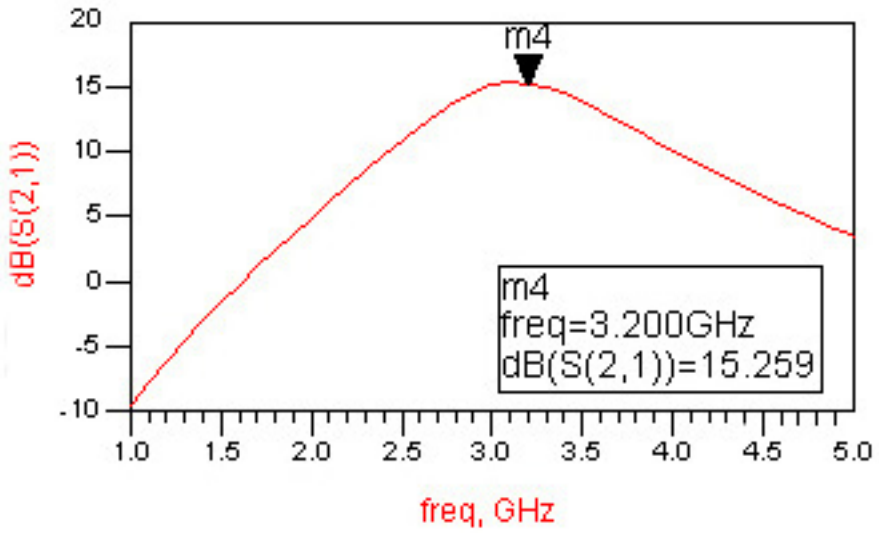
GOAL

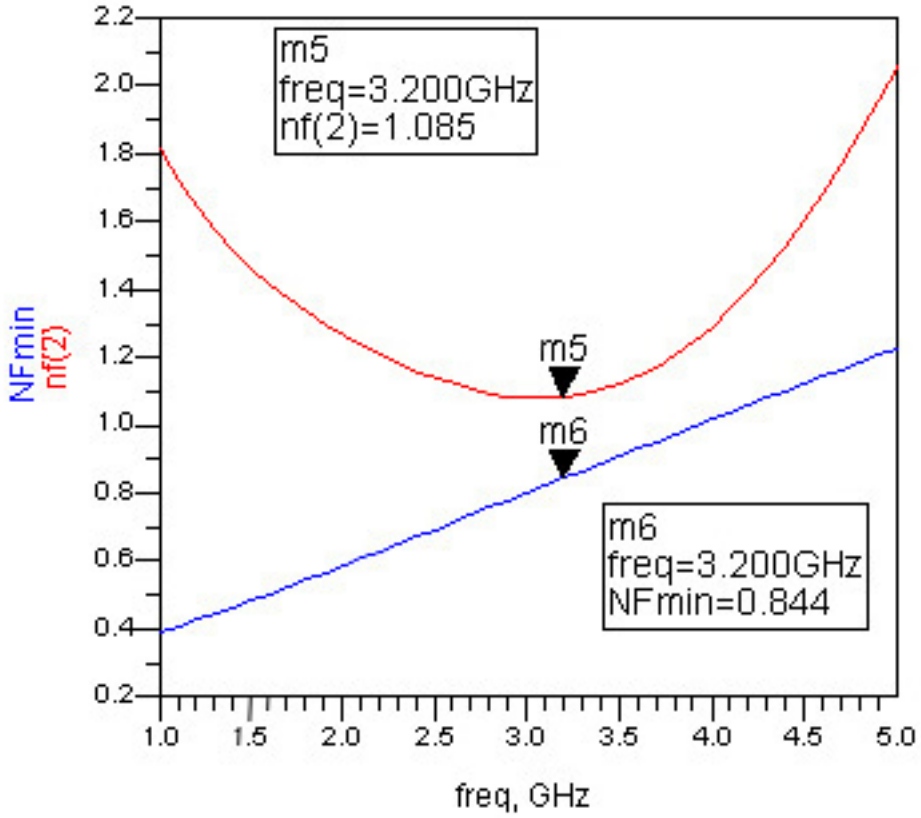
Goal
OptimGoal8
Expr="Power_mW"
SimInstanceName="DC1"
Min=
Max=60
Weight=3
RangeVar[1]=
RangeMin[1]=
RangeMax[1]=


0
-10
-20
-30
-40
dB(S(1,1))
m1
freq=3.200GHz
dB(S(1,1))=-31.986
m1
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
freq, GHz

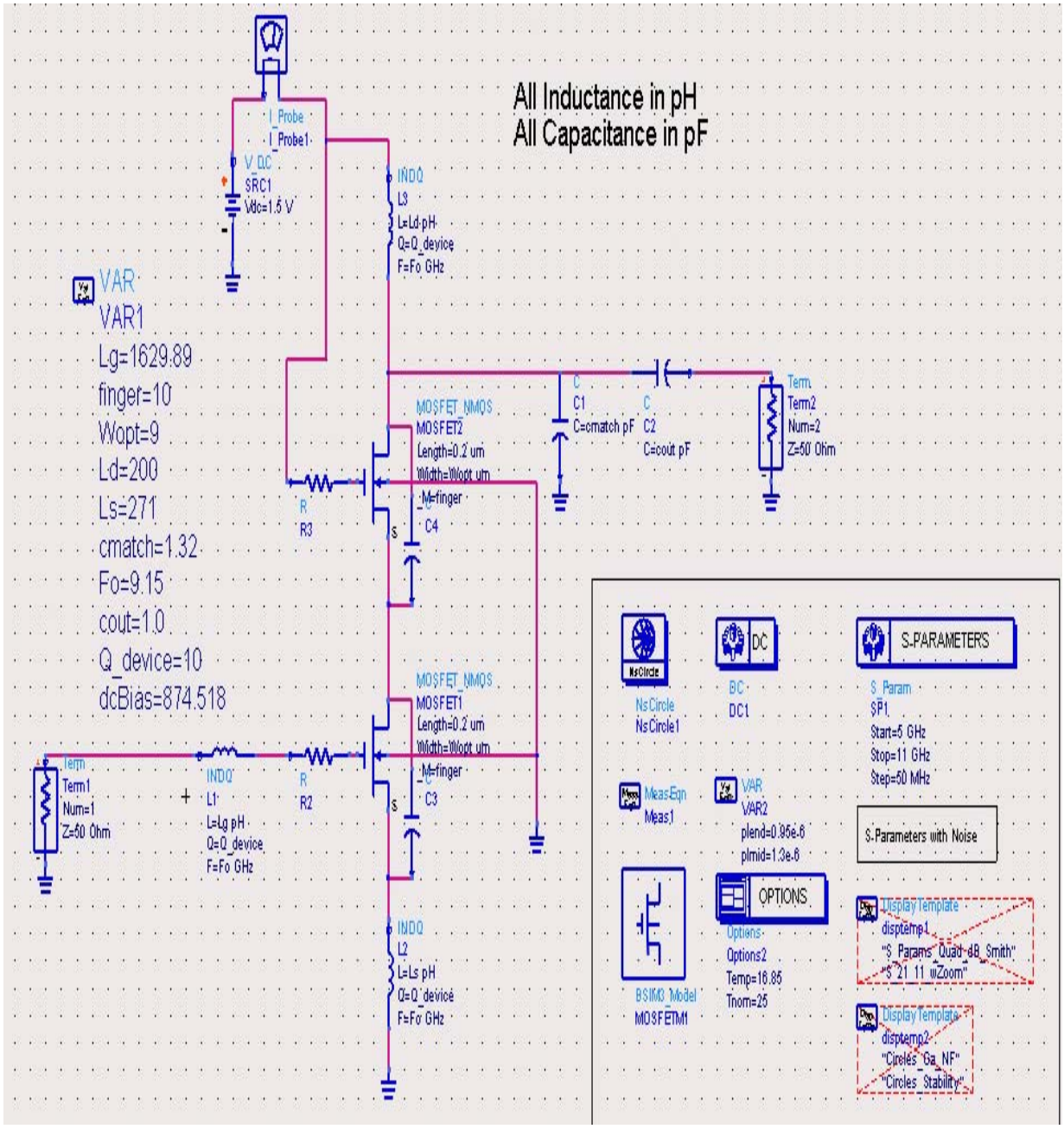

0
-5
-10
-15
-20
dB(S(2,2))
m2
freq=3.200GHz
dB(S(2,2))=-15.053
m2
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
freq, GHz

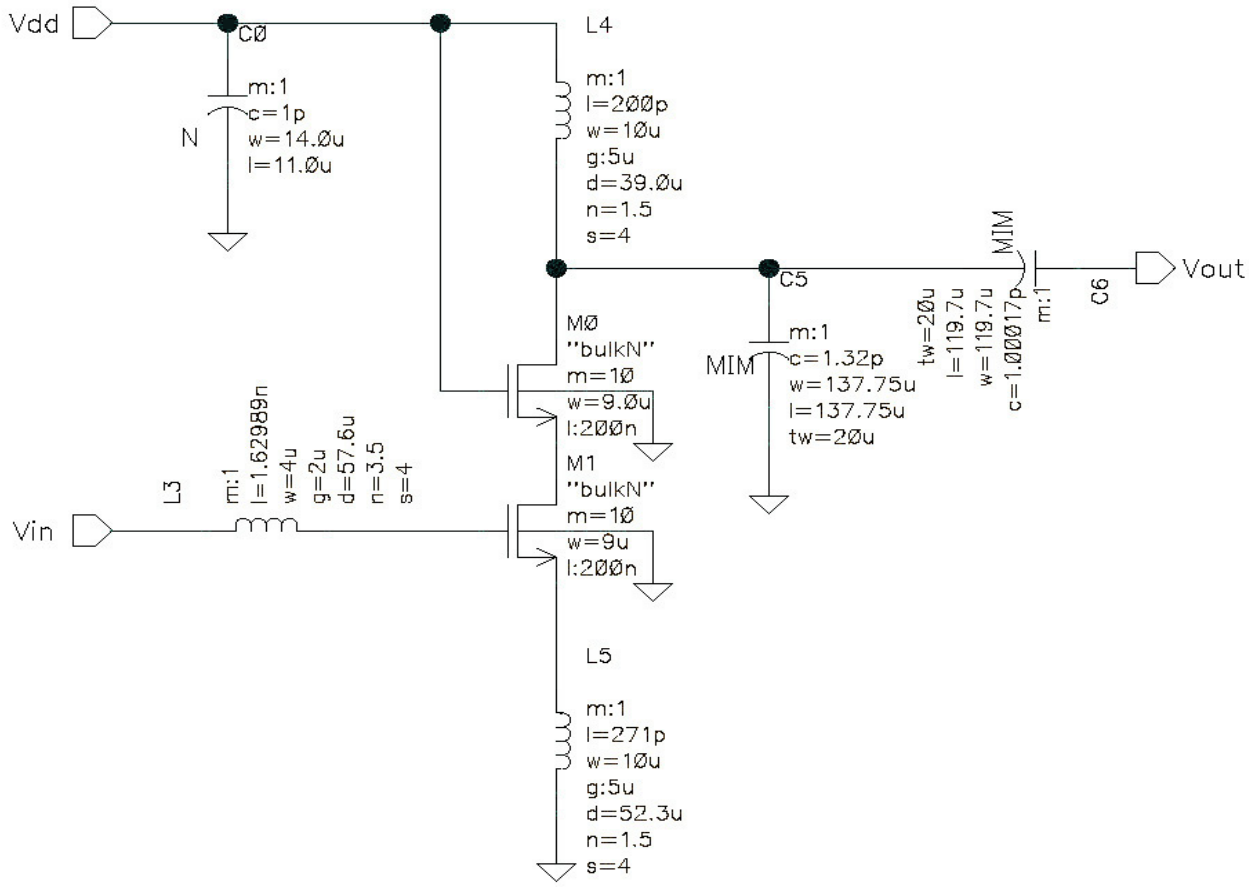

m3
-.30
-.40
-.50
-.60
-.70
dB(S(1,2))
m3
freq=3.200GHz
dB(S(1,2))=-31.627
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
freq, GHz

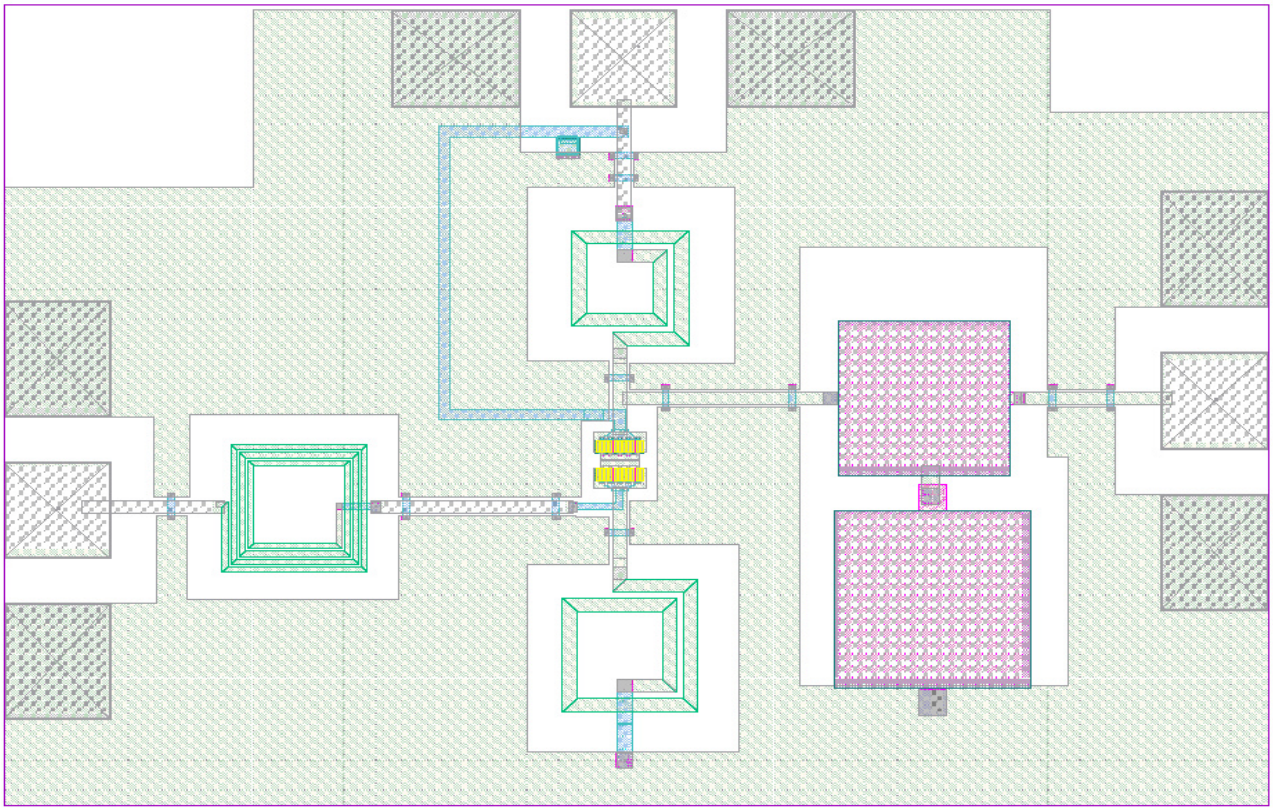

m4
20
15
10
5
0
-5
-10
dB(S(2,1))
m4
freq=3.200GHz
dB(S(2,1))=15.259
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
freq, GHz

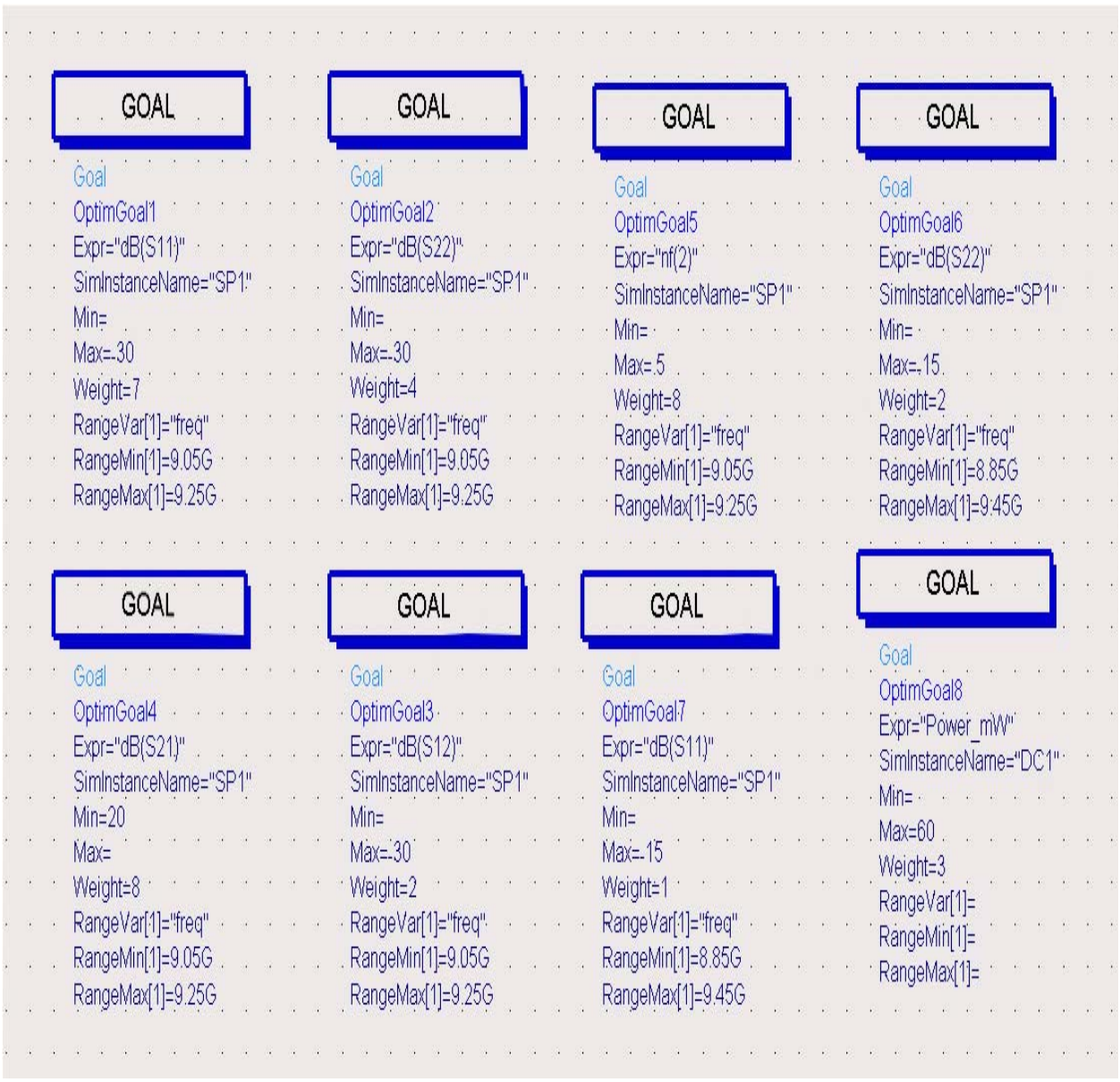


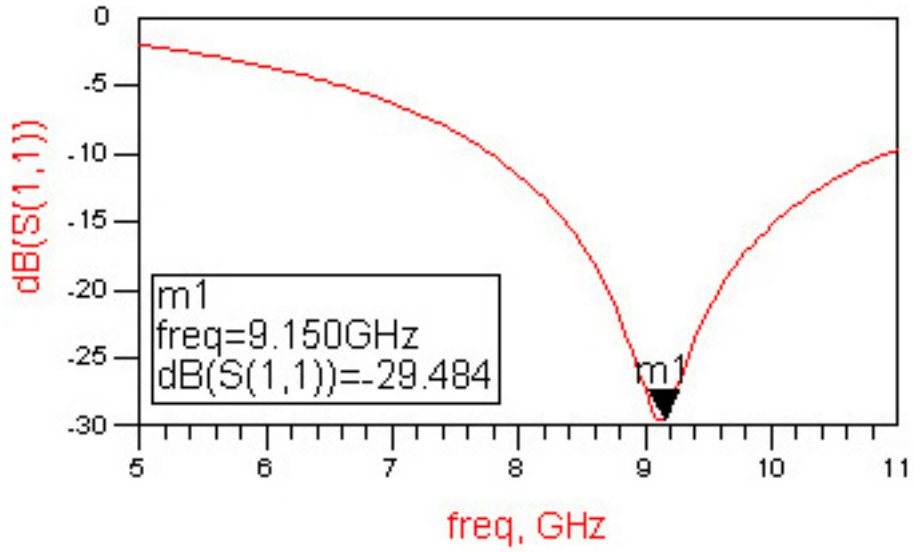
The X-band LNA has a center frequency of 9.15 GHz.

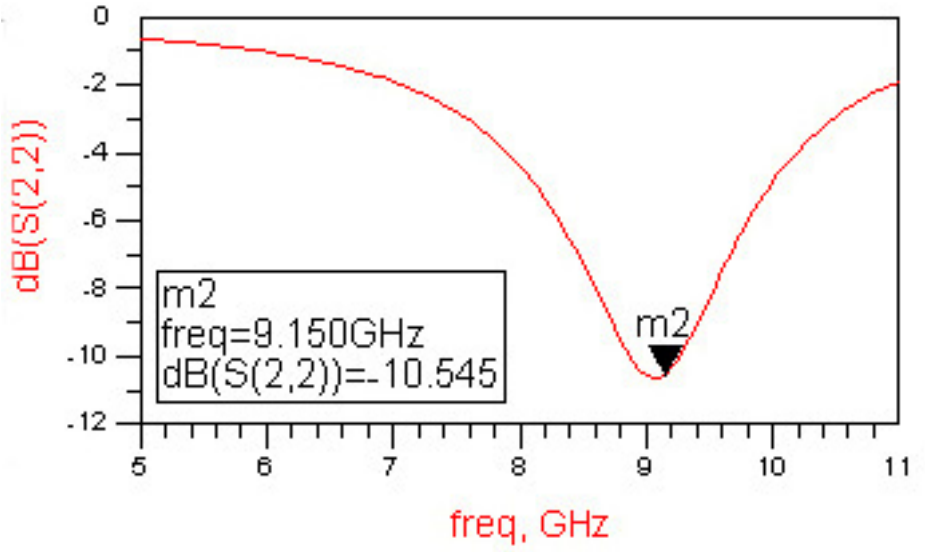

All Inductance in pH
All Capacitance in pF
I_Probe
I_Probe1
V_DC
SRC1
Vdc=1.5 V
INDQ
L3
L=Ld pH
Q=Q_device
F=Fo GHz
VAR
VAR1
Lg=1629.89
finger=10
Wopt=9
Ld=200
Ls=271
cmatch=1.32
Fo=9.15
cout=1.0
Q_device=10
dcBias=874.518
MOSFET_NMQS
MOSFET2
Length=0.2 um
Width=Wopt um
M=finger
C4
C
C1
C=cmatch pF
C
C2
C=cout pF
Term
Term2
Num=2
Z=50 Ohm
R
R3
MOSFET_NMQS
MOSFET1
Length=0.2 um
Width=Wopt um
M=finger
C3
Term
Term1
Num=1
Z=50 Ohm
INDQ
L1
L=Lg pH
Q=Q_device
F=Fo GHz
R
R2
INDQ
L2
L=Ls pH
Q=Q_device
F=Fo GHz
NsCircle
NsCircle1
DC
DC1
S-PARAMETERS
S_Param
SP1
Start=5 GHz
Stop=11 GHz
Step=50 MHz
MeasEqn
Meas1
VAR
VAR2
plend=0.95e-6
plmid=1.3e-6
S-Parameters with Noise
OPTIONS
Options
Options2
Temp=16.85
Tnom=25
DisplayTemplate
disptemp1
"S_Params_Quad_dB_Smith"
"S_21_11_wZoom"
BSIM3_Model
MOSFETM1
DisplayTemplate
disptemp2
"Circles_Ga_NF"
"Circles_Stability"

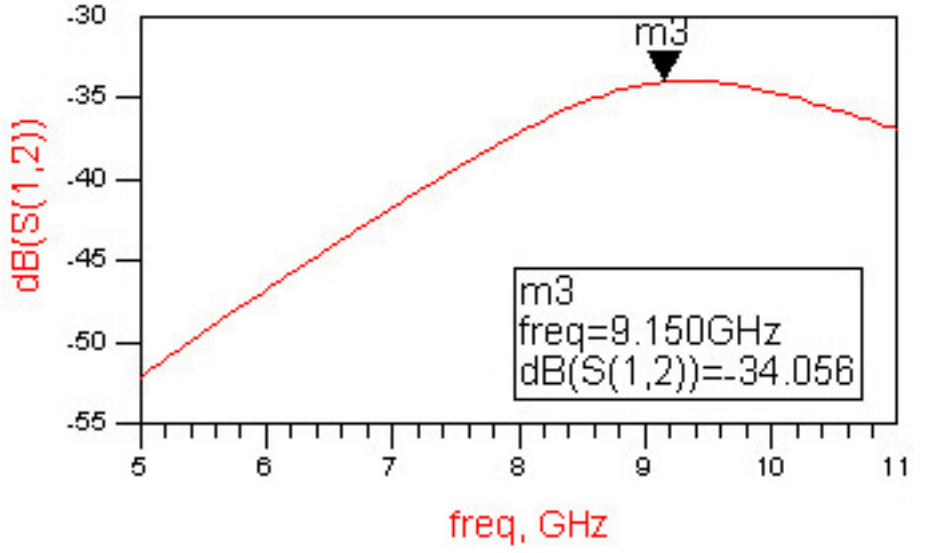

Vdd
C0
m:1
c=1p
w=14.0u
l=11.0u
N
L4
m:1
l=200p
w=10u
g:5u
d=39.0u
n=1.5
s=4
C5
MIM
m:1
c=1.32p
w=137.75u
l=137.75u
tw=20u
MIM
tw=20u
l=119.7u
w=119.7u
c=1.00017p
m:1
C6
Vout
M0
"bulkN"
m=10
w=9.0u
l:200n
M1
"bulkN"
m=10
w=9u
l:200n
L3
m:1
l=1.62989n
w=4u
g=2u
d=57.6u
n=3.5
s=4
Vin
L5
m:1
l=271p
w=10u
g:5u
d=52.3u
n=1.5
s=4

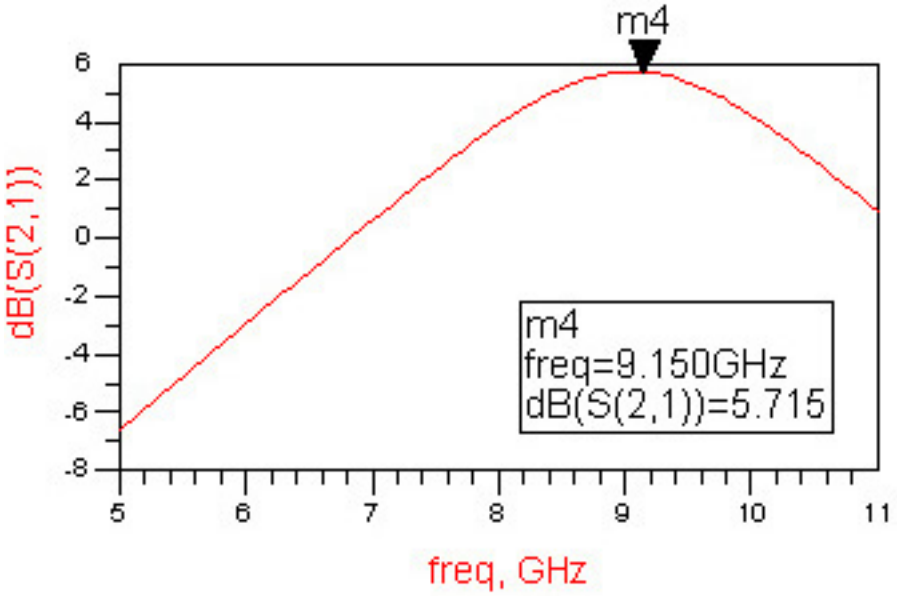


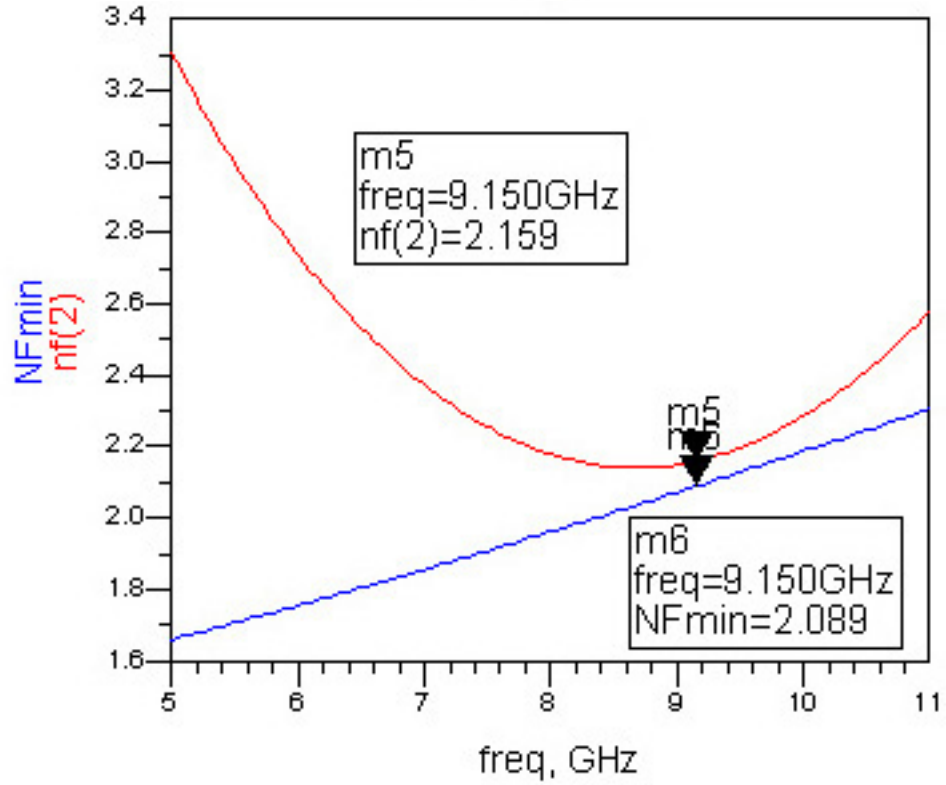

GOAL
Goal
OptimGoal1
Expr="dB(S11)"
SimInstanceName="SP1"
Min=
Max=-.30
Weight=7
RangeVar[1]="freq"
RangeMin[1]=9.05G
RangeMax[1]=9.25G
GOAL
Goal
OptimGoal2
Expr="dB(S22)"
SimInstanceName="SP1"
Min=
Max=-.30
Weight=4
RangeVar[1]="freq"
RangeMin[1]=9.05G
RangeMax[1]=9.25G
GOAL
Goal
OptimGoal5
Expr="nf(2)"
SimInstanceName="SP1"
Min=
Max=.5
Weight=8
RangeVar[1]="freq"
RangeMin[1]=9.05G
RangeMax[1]=9.25G
GOAL
Goal
OptimGoal6
Expr="dB(S22)"
SimInstanceName="SP1"
Min=
Max=-.15
Weight=2
RangeVar[1]="freq"
RangeMin[1]=8.85G
RangeMax[1]=9.45G
GOAL
Goal
OptimGoal4
Expr="dB(S21)"
SimInstanceName="SP1"
Min=20
Max=
Weight=8
RangeVar[1]="freq"
RangeMin[1]=9.05G
RangeMax[1]=9.25G
GOAL
Goal
OptimGoal3
Expr="dB(S12)"
SimInstanceName="SP1"
Min=
Max=-.30
Weight=2
RangeVar[1]="freq"
RangeMin[1]=9.05G
RangeMax[1]=9.25G
GOAL
Goal
OptimGoal7
Expr="dB(S11)"
SimInstanceName="SP1"
Min=
Max=-.15
Weight=1
RangeVar[1]="freq"
RangeMin[1]=8.85G
RangeMax[1]=9.45G
GOAL
Goal
OptimGoal8
Expr="Power_mW"
SimInstanceName="DC1"
Min=
Max=60
Weight=3
RangeVar[1]=
RangeMin[1]=
RangeMax[1]=


dB(S(1,1))
0
-5
-10
-15
-20
-25
-30
5
6
7
8
9
10
11
freq, GHz
m1
freq=9.150GHz
dB(S(1,1))=-29.484
m1


dB(S(2,2))
0
-2
-4
-6
-8
-10
-12
5
6
7
8
9
10
11
freq, GHz
m2
freq=9.150GHz
dB(S(2,2))=-10.545
m2


dB(S(1,2))
-30
-35
-40
-45
-50
-55
5
6
7
8
9
10
11
freq, GHz
m3
freq=9.150GHz
dB(S(1,2))=-34.056
m3





freq	Power_mW	I_Probe1.i
0.0000 Hz	21.920	14.61mA

Ed Murphy prepared a set of Matlab programs to compare simulation results of the OSU LNA design with measured results. The Matlab code is able to input the file format used by the test setup at WPAFB and compare it to the file format used by the simulation results from the ADS CAD tools. A sample of the code is included next.

```
clear
close all

% Loading the S-band LNA simulation data and assign to variables
[Ssim_S11freq Ssim_S11dB] = textread('LnaS_S11.dat','%f %f',...
'headerlines',1);
[Ssim_S12freq Ssim_S12dB] = textread('LnaS_S12.dat','%f %f',...
'headerlines',1);
[Ssim_S21freq Ssim_S21dB] = textread('LnaS_S21.dat','%f %f',...
'headerlines',1);
[Ssim_S22freq Ssim_S22dB] = textread('LnaS_S22.dat','%f %f',...
'headerlines',1);
[Ssim_NFfreq Ssim_NFdB] = textread('LnaS_NF.dat','%f %f',...
'headerlines',1);
[Ssim_NFminfreq Ssim_NFmindB] = textread('LnaS_NFmin.dat','%f %f',...
'headerlines',1);


% Loading the S-band LNA measured data and assign to variables
[Smeasured_S11freq Smeasured_S11dB] = textread('LnaS_S11meas.dat','%f %f',...
'headerlines',1);
[Smeasured_S12freq Smeasured_S12dB] = textread('LnaS_S12meas.dat','%f %f',...
'headerlines',1);
[Smeasured_S21freq Smeasured_S21dB] = textread('LnaS_S21meas.dat','%f %f',...
'headerlines',1);
[Smeasured_S22freq Smeasured_S22dB] = textread('LnaS_S22meas.dat','%f %f',...
```

```
'headerlines',1);
[Smeasured_NFfreq Smeasured_NFdB] = textread('LnaS_NFmeas.dat','%f %f',...
'headerlines',1);
[Smeasured_NFminfreq Smeasured_NFmindB] = textread('LnaS_NFminmeas.dat','%f %f',...
'headerlines',1);

DesignFreq = 3.2E9;

S_S11diff = Smeasured_S11dB - Ssim_S11dB;
S_S12diff = Smeasured_S12dB - Ssim_S12dB;
S_S21diff = Smeasured_S21dB - Ssim_S21dB;
S_S22diff = Smeasured_S22dB - Ssim_S22dB;
S_NFdiff = Smeasured_NFdB - Ssim_NFdB;
S_NFmindiff = Smeasured_NFmindB - Ssim_NFmindB;

% The figure Position property does not include the window borders,
% so here we define them with a width of 5 pixels on the sides and bottom and 30 pixels on the
top.
bdwidth = 5;
topbdwidth = 30;
% Ensure root units are pixels and get the size of the screen set(0,'Units','pixels')
scnsize = get(0,'ScreenSize');
% Define the size and location of the figures
% Position [left bottom width height]
pos1 = [bdwidth,1/3*scnsize(4) + bdwidth,scnsize(3)/1 - 2*bdwidth,scnsize(4)/1.5 - (topbdwidth
+ bdwidth)];
pos2 = [pos1(1) + scnsize(3)/25,pos1(2)/5,pos1(3),pos1(4)];

figure('Name','S-band Measured vs. Simulated','Position',pos2)
subplot(2,3,1), plot(Ssim_S11freq,S_S11diff)
title('S-band S11');
```

```
ylabel('dB');
xlabel('Frequency');
axis tight
% Mark minima and maxima
diffmin1 = find(min(S_S11diff) == S_S11diff);% Find the index of the min and max
diffmax1 = find(max(S_S11diff) == S_S11diff);
if Ssim_S11freq(diffmin1)< (min(xlim)+((max(xlim)-min(xlim))/2))
 HAmn1 = 'left';
 Txmn1 = (max(xlim)-min(xlim))/50;
else
 HAmn1 = 'right';
 Txmn1 = -(max(xlim)-min(xlim))/50;
end
if Ssim_S11freq(diffmax1)< (min(xlim)+((max(xlim)-min(xlim))/2))
 HAmx1 = 'left';
 Txmx1 = (max(xlim)-min(xlim))/50;
else
 HAmx1 = 'right';
 Txmx1 = -(max(xlim)-min(xlim))/50;
end
S_S11NegDiffFreq = Ssim_S11freq(diffmin1)
S_S11NegDiffdB = S_S11diff(diffmin1)
S_S11PosDiffFreq = Ssim_S11freq(diffmax1)
S_S11PosDiffdB = S_S11diff(diffmax1)
text(Ssim_S11freq(diffmin1)+Txmn1,S_S11diff(diffmin1)+(max(ylim)-min(ylim))/10,...
 ['Greatest Neg Diff = ',num2str(S_S11diff(diffmin1))],...
 'VerticalAlignment','bottom',...
 'HorizontalAlignment',HAmn1,...
 'FontSize',8,'EdgeColor','red');
text(Ssim_S11freq(diffmax1)+Txmx1,S_S11diff(diffmax1)-(max(ylim)-min(ylim))/20,...
['Greatest Pos Diff = ',num2str(S_S11diff(diffmax1))],...
```

```
 'VerticalAlignment','top',...
 'HorizontalAlignment',HAmx1,...
 'FontSize',8,'EdgeColor','red');

subplot(2,3,2), plot(Ssim_S12freq,S_S12diff)
title('S-band S12');
ylabel('dB');
xlabel('Frequency');
axis tight
% Mark minima and maxima
diffmin2 = find(min(S_S12diff) == S_S12diff);% Find the index of the min and max
diffmax2 = find(max(S_S12diff) == S_S12diff);
if Ssim_S12freq(diffmin2)< (min(xlim)+((max(xlim)-min(xlim))/2))
 HAmn2 = 'left';
 Txmn2 = (max(xlim)-min(xlim))/50;
else
 HAmn2 = 'right';
 Txmn2 = -(max(xlim)-min(xlim))/50;
end
if Ssim_S12freq(diffmax2)< (min(xlim)+((max(xlim)-min(xlim))/2))
 HAmx2 = 'left';
 Txmx2 = (max(xlim)-min(xlim))/50;
else
 HAmx2 = 'right';
 Txmx2 = -(max(xlim)-min(xlim))/50;
end
S_S12NegDiffFreq = Ssim_S12freq(diffmin2)
S_S12NegDiffdB = S_S12diff(diffmin2)
S_S12PosDiffFreq = Ssim_S12freq(diffmax2)
S_S12PosDiffdB = S_S12diff(diffmax2)
text(Ssim_S12freq(diffmin2)+Txmn2,S_S12diff(diffmin2)+(max(ylim)-min(ylim))/10,...
```

```
 ['Greatest Neg Diff = ',num2str(S_S12diff(diffmin2))],...
 'VerticalAlignment','bottom',...
 'HorizontalAlignment',HAmn2,...
 'FontSize',8,'EdgeColor','red');
text(Ssim_S12freq(diffmax2)+Txmx2,S_S12diff(diffmax2)-(max(ylim)-min(ylim))/20,...
['Greatest Pos Diff = ',num2str(S_S12diff(diffmax2))],...
 'VerticalAlignment','top',...
 'HorizontalAlignment',HAmx2,...
 'FontSize',8,'EdgeColor','red');
```

Ed Murphy exercised the automatic document generation feature of ADS for the LNA designed in the MP6 MITLL FDSOI process. The document generation capability will be useful for generating the types of specifications needed in the VSIA Extension documents. Ed Murphy and Jason Parry set up parasitic extractions of the LNA so as to have further simulations to compare to the test results. They synchronized the same transistor model for use in both the ADS and Cadence Spectre simulators.

B. RF/Analog Re-use and Analog Firm

This section of the report describes the work done for a design re-use design flow for RF/Analog and Mixed Signal. The work involved working with members of the Virtual Socket Interface Alliance (VSIA), an industry organization to facilitate the use of Integrated Circuit (IC) Intellectual Property (IP). VSIA facilitates the use of IP by developing standards for delivery of IC IP. These standards are embodied in documents and manuals referred to as Extension Specifications, since the delivery of IP often amounts to adding specifications to the original specification of the IC module being exchanged between the IP provider (seller) and the IP integrator (customer). The section describes the work effort in approximately chronological order.

We initially reviewed the VSIA Signal Integrity Extension Specification document as an example. The Signal Integrity document contains many requirement and specification

deliverables for design reuse. The issue for DoD will be how much of the extra work to produce these design content deliverables is warranted and how they should be modified to incorporate results from the NeoCAD program.

Initial review of the Mixed Signal chapter in the public domain VSIA based book “Surviving the SoC Revolution – A Guide to Platform Based Design,” by Henry Chang and Larry Cooke (Executive Director of VSIA) revealed public domain statements of many of the VSIA strategies for design re-use; in particular, the definition of “firm IP” for mixed signal design is extensively discussed.

Steve Bibyk coordinated with Raminderpahl Singh on the development of a framework for Analog/RF firm IP to take advantage of the synthesis tools and design test cases being developed under the DARPA NeoCAD program and to join Analog/RF circuit synthesis with system design for a receiver on a chip goal. We are evaluating whether the HDL language constructs used for digital design can be joined with some HDL constructs that would compatible with the NeoCAD tool flows. A planning write up of the effort is given next, along with new curriculum development to bring the content into graduate courses.

HDL-AMS constructs for mixed signal synthesis.

Recently, several mixed signal synthesis commercial CAD packages have become available, able to produce mixed signal VLSI layout from high level descriptions. Due to the nature of analog design, these CAD packages do not use HDL-AMS, (either VHDL-AMS or verilog-ams) as a starting point for the synthesis design flow. Instead, a performance goal script is used along with an initial captured design, usually at the structural level and in schematic or netlist form. The performance goal script is used in conjunction with test benches that are captured along with the structural design, so as to use some type of simulation-in-the-loop optimization procedure for the synthesis process.

On the other hand, the digital synthesis flow portion of a mixed signal design can be dramatically different from the analog synthesis portion. Digital synthesis is more amenable to using behavior

descriptions as the high level description for synthesis, in either VHDL or Verilog form, and often do not need testbenches/simulations to produce the initial synthesis results. Even when using critical path timing constraints, or physically knowledgeable synthesis, digital synthesis typically uses look up tables of delays rather than simulation-in-the-loop methods.

The main goal of this research is to develop HDL constructs that bring the analog and digital synthesis flow into a unified process. The research output will be high level descriptions that are able to be compiled and transformed into either verilog-ams or VHDL-AMS descriptions for the appropriate analog and digital synthesis processes. For analog synthesis, the HDL-AMS descriptions will include the performance goal scripts, testbenches, and foundry design kits necessary for the analog synthesis process. For digital synthesis, the output descriptions will include a cell based library in the same foundry process that is used for the analog synthesis. The final result will be a complete synthesis flow for system IC designs that use both analog and digital components.

A new course was developed at OSU with regards to the research program and is outlined next:

Hierarchical Design, Capture, and Verification of Mixed Signal Systems.

Objectives

1. Learn the advanced principles of combining analog and digital simulation strategies for design and verification of mixed signal systems.
2. Develop capabilities in using modern CAD tools for complete system design: initial specifications to manufactureable descriptions.

Texts:

Analog Behavioral Modeling with the Verilog-A Language by Fitzpatrick & Miller Verilog-A Users Manual, Cadence Design Tools.

1. Introduction, overview of mixed signal system design flow, analog design flow, course plan.
2. Mixed Signal System Descriptions and Simulations. Joint Spice and HDL Simulation Strategies.
3. Top down design with bottom up verification flows.

4. Mixed Signal Testbenches Analog verification vs. Digital verification.
5. Project Formation.
6. Basic Examples: Common Source Amplifiers, Inverters, Logic Gates Basic Op Amp, Flip Flops, Data Busses Voltage Regulators.
7. Application Examples: Error Correcting and Reconfigurable Data Converters. PLLs and Communication Transceivers.
8. Project Presentations

The VSIA Kickoff meeting report

The Analog Firm project is a Virtual Socket Interface Alliance (VSIA) Sub Group under the Implementation Development Working Group (DWG) (chaired by Raminderpal Singh). The Implementation DWG focuses on implementation and verification strategies for system chip design.

The goal of the Analog Firm project is to develop specifications for reuse and IP (Intellectual Property) databasing of analog/mixed signal circuits that is a cross between soft IP typical of digital designs and hard IP typical of analog designs.

Steven Bibyk at the Ohio State University is the chair of the sub group working on the Analog Firm project.

Meeting notes for Analog Firm Kickoff Meeting Wed. Feb. 11 2004

Present:
Raminderpal Singh, Juan-Antonio Carballo, Sonal Venkatadri, Mar Hershenson, Navraj Nandra, Henry Chang, Raj Nair, Steve Bibyk

Mazen Allawi stepped out.

A round table discussion was had on what folks thought the content would be for the white paper. These notes are divided into 3 parts. Part I is the notes on the specific issues of:

a) What makes up Analog Firm
b) Audience and c) Purpose of white paper

Part Two is a recap of comments made during the meeting. Part Two needs to be reviewed to pull out the main sub themes of the paper, given that Analog Firm is the main theme. Part III lists next steps.

Part I

a) Analog Firm:

- Generally, it's IP bound to a technology.
- Must be deployable.
- May include layout, schematics, encoded functional description, etc.
- Analog Firm is closer to Analog Hard than Analog Soft
- HDL descriptions tend toward Analog Soft, but do help reuse via design documentation.
- Simulation Testbenches along with design objectives and constraints.
- Somewhat process independent.
- Firming up content to get to layout. High level abstraction models and content that leads to LVS-ready netlists.
- 'Firm' connotes something that is unchanging and in that sense, Analog Firm IP could be a set of oft-required, integrateable analog functional blocks, of clearly specified electrical (or electromagnetic) function and input/output with a firm internal circuit architecture, associated with a physical layout optimal for the function, and associated with code capturing the analog intelligence that facilitates first-cut, reasonable process translations in automated tools.

Further Analog Firm concepts are in Part II - Recap of the Meeting Notes.

b) Audience:

- Analog/mixed signal design tool developers.
- Mixed-signal block designers.

- Mixed signal system designers and chip integrators.
- Design Automation Communities and forums.
- Analog Experts.
- System designers with need to speed up analog design flow portion.

c). Purpose:

- Define the problem "unambiguously" and bounds of the problem.
- (VSIA) standards development.
- Provide feedback on CAD tool needs and development.
- Generate enough output to lead to a full standards document.
- Specify content that a Provider of Analog Firm would deliver to a User.

Part II – Recap of Meeting

Summary of how Barcelona's CAD tools worked.

Algorithms used for sizing topologies and also for physical design. In physical design, there is need for sophisticated design kits. These tools exercise pcells in complex layout design creation.

Analog firm is design content that is in addition to schematics and layout that enables reuse of a design.

Objective of putting group together and getting content created. DAC deliverable, and how tools fit in the game.

DARPA NeoCAD program objective is to improve analog design flows for defense contractors designing high performance (but low volume) electronic systems.

Analog synthesis tools being developed from NeoCAD (and elsewhere) typically start out with a topology and the synthesis process produces schematic sizing and other related optimization (tuning and tweaking) procedures. In addition, the tools produce automated layouts via place and route algorithms and pcell instantiations.

There is another major aspect of analog IP which involves developing new topologies, especially as process technology improvements enable different architecture options to achieve significantly higher performance.

Discussion on the differences between Analog IP and Analog Firm.
Analog Firm could be content that facilitates production of schematics and layouts for a process migration. Analog Firm content is somewhat process independent, and includes system level concepts of objectives and constraints and is closer to Analog Hard rather than Analog Soft.

Some discussion on the use of language and constructs such as HDLs. HDLs tend to promote the idea of soft IP. The utility of Analog Soft IP is more ambiguous than that of Analog Firm IP.

Notion of firming up content to layout. High level abstraction models and content that leads to LVSable netlists.

HDLs are being used for mixed signal design. The digital portion of a mixed signal design is typically in an HDL design flow. Mentor's customers used HDL in developing system designs. Even if you don't use HDLs, you need some methods and language of describing what the design is about for later use. The default is schematic notes. The problem with schematics and their notes is that the content is very tool specific. Languages are much more portable across a wide variety of point tools. Designers capture design content after a design is nearly done to enhance its reuse, although this is extra work and it is difficult to specify in a priority matter what content is most valuable for reuse.

Many system designers use Matlab, Excel, or write c code.

One of the major issues with process migration of analog designs is the amount of rework needed in a design. If there were 100 cells that needed to be migrated and 70 of them could be done with minimal rework using some of the synthesis tools, then the analog design team could focus on the remaining 30 cells that would require intense hand crafting.

Analog firm concepts from the point of view of the provider vs. the user.
Large companies would have a different infrastructure for internal analog reuse than smaller companies.

Example of Broadcom and its large CAD group that enables porting of designs across different process technologies.
Smaller companies can't afford this type of CAD group and CAD tool investment. On the other hand, if the small company was an analog IP provider, then the CAD tools use might be similar to that of a large company.

Two types of content for reuse.
One was models to evaluate at the system level and assist the integration process and evaluate the designs at the system level without notions of layout. The second was content that would be used for cell synthesis and that would enable implementation and process migration.

Content that is needed to integrate cells together that would help facilitate design review concerns, such as substrate noise, cell boundaries, etc.

Audience.
Need to motivate the limited group of analog experts to produce the content to fill the skeleton structure of analog firm. A larger audience is all the designers that need to include analog content but are analog apprentices, (although maybe skilled at chip integration with hardware/software codesign).

Extensive and high value design kits are one method of increasing analog reuse such as to have more elaborate pcells that allow a previous schematic to reach layout quickly.

Wrap up discussion to achieve some specific outputs to the following:
1) What makes up Analog Firm? 2) Who is our audience, and what is the purpose of the document, and 3) What are the key thrust areas of discussion or what will be the major themes of the document?

Part III

Next Steps.

There is sufficient content to finalize the short descriptions of Analog Firm, Audience, and Purpose. Since analog and mixed signal design is a complex and diverse topic, the finalized short descriptions can be used to keep the discussion and content development on track.

- Schedule a conference call for around Wednesday afternoon, March 10.

- Develop a set of Specifications that allow smaller companies to figure out an analog reuse procedure that is similar to what larger companies do internally. Smaller companies would buy Analog Firm content and would firm up the content in a market-timely manner (using various tools and procedures) to layout and tape out form.

The terms large company and small company are synonyms for an analog internal reuse company vs. a company that would externally reuse (i.e., buy analog firm IP). Of course, a large company could buy analog IP and a small company could be an internal reuser.

- Reference material. The Design Automation chapter in R. Singh et al. Silicon Germanium book has useful material. In particular, section 3.2 on synthesis of ESD – Best Practice CAD implementation, is an example of an internal reuse strategy that is being somewhat shared with IBM customers. (Provider to User).

Steve Bibyk contacted the individual members of the VSIA Analog Firm working group and set up tasks for the next conference call, which was on April 29. The minutes are given next. The development of the Analog Firm specifications can be a useful set of design methodologies for a mixed signal design center that needs to organize and database design content and design libraries.

The Analog Firm group will meet up at DAC in San Diego. Possible meeting times are Tuesday evening during the PhD forum, the Wednesday lunch break, or Thursday afternoon to evening. Steve Bibyk is attending the DAC Friday tutorial on Automated Macromodeling for Mixed

Signal Design. Some Analog Firm discussion may take place in that tutorial. Juan-Antonio Carballo is one of the tutorial presenters and a member of the Analog Firm group.

Initial notes for Analog Firm 2nd Meeting Thurs. April 29, 2004

Present:

Mazen Allawi, Juan-Antonio Carballo, Mar Hershenson, Navraj Nandra, Henry Chang, Raj Nair, Steve Bibyk

Agenda:

1. Develop outline of the white paper.
2. Plan to meet at upcoming DAC to review draft of white paper.
3. Discussion of writing tasks.
4. Next conference call in a couple of weeks.

Actions:

Everyone will email out their possible times for meeting at DAC.

Steve – will draft intro and outline, send out context framework for the content received so far. Contact Sonal and Raminderpahl.

Navraj – modify writing for context and present Barcelona design point of view. How design kits are improving to be used with the Barcelona type tools.

Mar – will discuss how sophisticated (hierarchical) p cells are used with optimizers.

Raj – will talk about how a design firm delivers IP and how a designer might leave behind some content that future designers at the client could use. (What types of simulations should be run, what types of bugs and errors to watch out for, what are the nuances of layout effects).

Juan-Antonio - write about how IP is bound to a technology and what the binding mechanisms are. If it was unbound from one technology and bound to the next, what would be the binding

entities? VSIA standards development. What makes up a good design kit that improves mixed signal productivity and helps analog firm along.

Henry – sent George Powley's paper and expand on the notion of improving verification, more time on verification means less time on entry and capture of the construction parts of the design.

Mazen - will write about things from a traditional point of analog IP point of view and also what they would like to see in design kits that help their IP work.

Sonal – what makes up a design kit?
Now that Cadence has purchased Neolinear, how will IBM change their design kit so that it works better with the Cadence tool flow?

Outline of Analog Firm Whitepaper

I Introduction (Steve, Raminderpahl, …)

Analog IP – Design descriptions that have re-use capability. It is difficult to specify and put bounds on the problem. Analog abstraction methods are significantly different than digital abstraction methods, but where both methods are similar, there should be similar design flows.

Hard IP - GDS2 Layouts plus component verification model. Both fixed.
Firm IP – Capability to modify/generate layouts and modify component models, plus other design content.

Customer of Firm IP is given mechanisms to perform above modifications by the Firm IP vendor. Mixed signal design community needs specifications of those mechanisms in the context of a mixed signal design flow and these specifications need to be developed in a VSIA Extension document.

Contributions to the Specifications: 1. EDA vendors, 2. Designers, 3. Foundries

Analog Firm - What's new, what's different, what's better?

Synthesis is farther along.

Summarize Analog Firm from past publications, preview Analog Firm as discussed in this document, and add some limited predictions of future development in Analog Firm.

II. EDA Vendors (Navraj, Mar, Henry)

New developments in mixed signal design flows.

Mixed signal testbenches enhance ability to develop physically based optimization that can be linked to layout generation.

Design descriptions above the schematic level – Verification methods used to explore a design development are an aspect of high level synthesis.

III. Designers (Juan-Antonio, Raj, Mazen)

Connecting Firm IP to a technology.

Packaging and selling design methods that are not inherent in CAD tools.

Experiences in selling Analog IP.

IV. Foundry Design Kits (Sonal, Mazen, Raminderpahl)

Increasingly sophisticated parameterized cells and accurate model development are enhancing physically based synthesis methods.

V. Contents of an Analog Firm Specification Extension (All)

VI. Conclusions

Some summary items from the results of the Analog Firm meetings at DAC are given next:

1. VSIA leadership of the Analog Firm group is now done by Juan Antonio Carballo, a mixed signal system architect at IBM, Austin, TX. VSIA has also reorganized to be more responsive to its membership, setting up three main thrusts in IP Quality, IP Protection, and IP R&D. J. Carballo is the director of the IP R&D thrust. Steve Bibyk is still the integrator for the Analog Firm work.

2. The VSIA activity will be correlated with the OpenAccess Database effort developed by the Silicon Integration Initiative (www.si2.com). This group is made up of users and developers of CAD tools, with the goal that all the CAD tools should use the same database. This allows users to integrate their own tool flows and to allow straightforward comparisons of CAD tools on the same design. For example, in the NeoCAD program, Neolinear used the OpenAccess Database, but other programs did not.

Working draft of the Analog Firm program.

I Introduction (Steve, Raminderpahl, …)

1. The Problem statement goes here. There can be a long list of reasons why Analog IP is needed. List the best ones here:

For example, the productivity gap continues to increase between the new fabrication processes and what can be designed in a timely manner.

2. The Solution Strategy goes here. There can be another long list why the need for Analog IP seems harder to satisfy than Digital IP. List the best ones here:

For example, list some factors that slow down or confuse the process to get to working mixed signal layout. Note possible steps that overcome these slow down factors.

Note that the productivity_gap/schedule pressure has increased to the level that even incremental solution measures being offered by the EDA vendors and foundries are useful. Therefore, methods that are more than an incremental improvement can be a major accomplishment.

The open kit initiative, launched in 2003, has online documents that list many of the usual issues with Analog IP, both the reasons why it's needed and why that need has a hard time being met. Although there is some content from EDA vendors and Designers point of view, the emphasis seems to be on the design kits.
http://www.eda.org/openkit/

Analog IP – Design descriptions that have re-use capability are difficult to specify and put bounds on the problem. Analog abstraction methods are significantly different than digital abstraction methods, but where both methods are similar, there should be similar design flows.

Hard IP - GDS2 Layouts plus component verification model. Both fixed.
Firm IP – Capability to modify/generate layouts and modify component models, plus other design content.

Business model of IP probably implies some aspect of information hiding. Hard IP hides too much information. The specifications for Firm IP should list the structure of the added information. There probably needs to be different levels of specification complexity: 1. Minimal, 2. Basic, 3. Thorough, 4. Comprehensive. The higher the complexity level, the more resources are needed to meet the specs. However, in some situations, the costs and time associated with the added complexity could undermine the main reason to use IP, such as design schedule improvement. This tradeoff seems more difficult to map out for Analog and/or RF IP than for Digital IP.

A customer of Firm IP is given mechanisms to perform above modifications by the Firm IP vendor. The mixed signal design community needs specifications of those mechanisms in the context of a mixed signal design flow and these specifications need to be developed in a VSIA Extension document.

Contributions to the Specifications: 1. EDA vendors, 2. Designers, 3. Foundries

Analog Firm - What's new, what's different, what's better?

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Summarize Analog Firm from past publications, preview Analog Firm as discussed in this document, and add some limited predictions of future development in Analog Firm.

II. EDA Vendors (Navraj, Mar, Henry)

New developments in mixed signal design flows.

Mixed signal testbenches enhance ability to develop physically based optimization that can be linked to layout generation.

Design descriptions above the schematic level – Verification methods used to explore a design development are an aspect of high level synthesis.

Sub-themes for white paper:

One suggestion is to consider "Successful Analog Firm IP Deployment"

Major issues to consider in this sub-theme would be:

1. Process, temperature, voltage variations
2. Inherent, substrate and supply noise
3. Careful layout techniques:
    - 3.1 Symmetry, device and block mismatches
    - 3.2 Parasitic and proximity effects
4. Hierarchical design: scalability and reuse
5. System Constraints

There are several reasons that make analog circuit design in an SoC a very complex task. First of all, analog circuit performance depends on the transistor behavior. Small variations in the manufacturing process can result in dramatic changes in circuit performance. This translates into a need for accurate transistor models over different process corners. Another important concern in mixed-mode ICs is substrate noise coupling. Fast switching digital circuitry can deteriorate significantly the value of the sensitive analog signals. Also careful layout to reduce device

mismatches and parasitics is crucial to guarantee correct circuit behavior. Finally, unlike digital circuits, the designer has to keep in mind a large number of performance specifications, making it time consuming to redesign an analog block.

Another important and overlooked issue is that an analog designer is required to create a new custom circuit or just perform new sizing of an already existing circuit. This design flow does not encapsulate the knowledge of this designer and as such it cannot be used later by a less experienced designer. For example, an experienced designer might know exactly what to tweak, change or be watchful of in a design. However, this information is not embedded anywhere so even if he has spent many months in a design, if he decides to leave the design group, most of that information is lost.

The completely different design schedules of analog and digital was not an issue when two separate parts were sold. Semiconductor companies would market a new chipset every time a new IC process was released (even though only the digital part had changed). Today, however, in order to take advantage of the new process technologies, semiconductor companies are forced to have comparable design schedules for both analog and digital. This is a big issue because of the tremendous difference in design efficiency between the analog and digital parts. While the design of digital circuits is highly automated, the design of analog circuits is still manual.

Regarding the Analog Firm audience, I would summarize into the following:

1. Analog CAD flow/methodology engineers

These are CAD engineers responsible for the introduction and integration of analog design flows into a mixed signal design flow. They are concerned about the analog simulators and simulation models available (BSIM, VBIC, MEXTRAM etc). Views available (symbol, schematic, HDL). Types of PCELL's: as well as NMOS and PMOS, bipolars may be needed and certainly resistors and capacitors are required. Are any special layers required to achieve isolation and low noise, for example NWELL and or guardrings. In fact their job is to ensure that they can provide all these requirements in a PDK consisting at least of software programs and libraries. The libraries contain full front end (symbol, schematic, simulation model). And back end (placement outlines, full layout) information for the development of digital and mixed signal circuits in one of the

major EDA platforms. The software programs can include, for example, parasitic device simulation and safe operating area check programs (very important in analog). I believe the analog CAD flow engineers to be providers of tools in order to firm the analog IP and getting feedback from the analog designers to ensure quality standards are met. The key question is: will my analog IP work (on silicon) once it is firmed up.

2. Analog in SoC designers

These are analog IC designers in companies like Broadcom. They are customers of the analog CAD flow engineers.

3. Merchant analog designer

These are the hardcore analog designers at Maxim or Linear Technology. They push performance to the limit and rely on tweaking the foundry process in order to meet performance. Probably not a good target for analog firm unless we can show a performance enhancement in terms of power saved, lower noise, lower offsets, higher bandwidths, higher Q's, etc.

III. Designers (Juan-Antonio, Raj, Mazen)

Connecting Firm IP to a technology.
Packaging and selling design methods that are not inherent in CAD tools.
Experiences in selling Analog IP.

A facility for easy exchange of intellectual property (IP), the lifeblood of commerce, will be of great benefit to startup companies, particularly in the analog and mixed-signal arena.

While developing end products based on analog IP facilitates the promotion of the IP, the cost of such development and the time taken for it adds substantially to the time-to-market and time-to-money (TTM) durations. However, if standardized means to capture the analog intelligence (structural algorithms accomplishing desired manipulations of continuous-time and continuous-value signals) were to be made available, startup and small companies could transfer their

concepts to interested customers for speedier implementation into a wider range of products, thereby enhancing the chances of success and proliferation of that IP.

Analog firm IP could hence be viewed as captured analog intelligence, which provides the necessary and sufficient information about an analog circuit, functional block, or system allowing for the implementation of the IP on an appropriate fabrication process technology. Due to the 'analog' nature of such an implementation, a number of function and performance-critical rules of implementation are also packaged within the IP form. Some of these implementation (physical or layout design) rules are generic enough that they may be incorporated as 'analog' rules within EDA tools, while some may be IP-specific. For example, most current-mirrors and amplifiers require matched transistors. Bandgap voltage references require matched diode implementations; high-bandwidth designs require certain device structures and placement that minimizes parasitic elements. IP-specific requirements may include device noise characteristics that may require devices of a certain size or matching of device parasitic values with external elements, etc.

Small companies work with corresponding budgets and it is not feasible for such companies to staff a large, skilled CAD team that can ensure speedy and efficient translation of analog firm IP into implementations on a fabrication process technology. Moreover, the inclusion into a CAD suite of the entire set of 'analog' rules (in specifications) to optimally implement any given analog IP may also not be feasible. An exhaustive, shotgun validation approach, or even a neural-net-based search for globally optimal design implementations may not be computationally feasible for most analog IP. It would seem, therefore, that while CAD tools may be enhanced to better serve the needs of analog design, some of the intelligence that would lead to an optimal implementation of a given analog IP would need to be included within the IP, in the form of executable or interpreted implementation code, or specifications in text and verification rules specific to the IP. This was the approach ComLSI adopted in providing inputs to an EDA company focused on tools for analog and mixed-signal design. Recommended analog enhancements [reference 1] to the physical design tools included the ability to:

- Match devices following known common-centroided and other matching techniques,

- Generate devices following ‘analog’ device topographical rules, and
- Provide real-time DRC checks assisting the speed-up of custom design

An example of IP-specific analog physical design is detailed in reference 2 in the implementation of a 4GHz internal clock distribution for a terabits/sec crossbar switch component. In this design, the main clock bus was implemented as split wires with shielding on multiple sides that reduced the overall effective RC of the clock bus substantially, thereby increasing its skew and jitter-minimizing shorting effectivity.

References

1. Raj Nair, “*Preliminary evaluation report on L-Edit™ V10.0,*” July 9, 2003 (unpublished).
2. Raj Nair, et al., “*A 28.5GB/S CMOS Non-Blocking Router for Terabits/S Connectivity between Multiple Processors and Peripheral I/O Nodes,*” Solid-State Circuits Conference, 2001. Digest of Technical Papers. ISSCC. 2001 IEEE International, 2001 Page(s): 224 -225, 450.

Analog IP History and trends

With more and more advanced technology and the continuous demand on shrinking size and increasing functionalities, SoC design is a major focus of the semiconductor world. This focus brings significant business pressure and opportunity for the Semiconductor Intellectual Property (SIP) market and, in the last 10 years, the SIP market has grown substantially. With the growing number of digital IPs available on the market in the past few years, designer teams have realized that analog functions are a bottle neck that prohibits deployment of high performance designs. Therefore, there is increased demand for analog SIPs. EDA vendors, foundries, and IP companies have offered new products to address the demand.

Historically, analog intellectual property was usually available through an IDM (Independent Device Manufacturer) and it was a take-it or leave-it type of business. The lack of analog design expertise in the industry has also made it difficult for designers to design and integrate analog IP

into the SoC. This trend in the market place is now changing. Today, with the emergence of a number of new companies specializing in analog design and functionality, Analog IP is finally beginning to gain the stature and increased attention within the semiconductor community.

A larger library of available analog functional blocks has emerged during the last several years. Analog IPs vendors are now providing more complicated and high performance PLL, DAC/ADC IPs instead of the basic functions several years ago. Most interestingly, high performance power management functions like voltage regulators and DC/DC converters, which were only available in discrete chip format from IDMs several years ago are now available in IPs that can be integrated into SoCs designed in state of the art CMOS technology.

While analog IP is experiencing a fast grow curve, there are several challenges that are facing analog designers. The first one is reusability. By nature of the analog design, it is highly process dependent. A different process technology, even the variation of the same process, will have a significant impact on the performance of an analog design. Therefore, analog blocks that are fully characterized and tested are most desirable for IP users. This requires the analog IP provider to invest in silicon fabrication and testing before talking to potential customers.

Another challenge is analog design automation. Digital designs are becoming half-automatic manufacturing, with the help from design automation vendors. Companies like Cadence have already provided different tools for different tasks in digital designs. However, analog designs, especially deep sub-micron analog IP designs are still a fine art.

With challenges and growing potential ahead, it’s up to these analog IP players to draw the growth curve in the next few years.

IV. Foundry Design Kits (Sonal, Mazen, Raminderpahl)

Increasingly sophisticated parameterized cells and accurate model development are enhancing physically based synthesis methods.

The open kit initiative, launched in 2003, has some useful detail buried in large discussion documents.

http://www.eda.org/openkit/

V. Contents of an Analog Firm Specification Extension (All)

VI. Conclusions

Analog Firm meeting at DAC and follow up

Steve Bibyk discussed the VSIA Analog Firm project with members of the VSIA group and also at the Automated Macromodelling for Complex Analog and Mixed-Signal Integrated Systems Workshop at DAC. The members of the group concluded that the Analog Firm white paper should have an end of the calendar year deadline. Juan-Antonio Carballo is now the main VSIA member of the group, being the director of the R&D pillar for VSIA.

The main conclusion from the discussion and the workshop is that system level synthesis will rely on macromodel techniques and that modeling for synthesis is different than modeling to predict measured results. The synthesis model parameters would be determined using similar optimization algorithms that are used for individual cell sizing, such as that used in Cadence NeoCell and Agilent ADS. However, the simulation templates for macromodeling are harder to establish than the simulation testbenches for individual cells. Nevertheless, macromodel simulation templates should be similar to the system simulations used to partition a system design and determine the performance requirements of the individual components. Such an approach could first be developed for an RF transceiver chain.

Discussions with the Director of R&D for VSIA on the next Analog Firm actions

Main action item is a group teleconference in September to coordinate the white paper content development from the members of the working group.

One of the main items needed for the white paper are examples of analog and RF testbenches (i.e., simulations scripts) that are used for design decisions, such as schematic sizing. These testbenches represent a form of IP which can be used to port the design from its initial requirements to a new set of requirements. One of the problems with a Cadence design flow is the difficulty in capturing the testbenches as easily documented files. This problem was somewhat addressed in the Neolinear approach to design templates and since Neolinear is now part of Cadence may permeate other aspects of the analog and RF Cadence design environment. However, the Neolinear templates were entered using a GUI approach with pull down menus, so it still needs to be determined whether these templates can be extracted as easily documented testbenches. The testbenches, along with macromodels of the design under test (DUT), would represent a form of Analog/RF IP that would enable a system integrator to insert the DUT and modify it based on system requirements. Such an approach would be similar to the Model Driven Architecture (MDA) methodology used for object design in software design and re-use.

Some updates on changes in the VSIA organization are in the following press release (Sept. 20, 2004) on the new board members. http://www.vsi.org/news/pressrelease/pr_092004.pdf. Note the recent activities in IP Quality and IP protection and that Analog Firm is being developed in the R&D pillar. There is also a good article on standards development linked from the VSIA web page to Electronic Business: http://www.reed-electronics.com/eb-mag/article/CA447600. Part of the article talks about the slowness with standards development when there are competing solutions, such as in the ultrawideband standards process. Lots of travel to a variety of meetings produced stalemate results. Our Analog Firm group also has aspects of competing solutions, but we have been very good about minimizing travel to meetings. Hopefully, that can continue as we put in the detailed content of the white paper.

Steve Bibyk talked with Juan Antonio, Mazen, Navraj, and Mar at DAC but was unable to meet with Henry Chang. Bibyk also talked with Anthony Gadient of Neolinear (now Cadence).

Bibyk and students attended the Automated Macromodeling Techniques for Complex Mixed Signal Systems Tutorial, where Juan Antonio gave an excellent presentation. During that all day tutorial, it seemed pretty clear that modeling methods were an important aspect of analog IP and

thus Analog Firm and there seems to be too little standardization in the model formats. Some of the presenters talked about using HDLs to develop standard models, but members of the audience pointed out that representing models in HDL is much extra work which slows down the actual development of the physical design formats. In fact, the CAD tools that I have seen to speed up analog physical design (schematic sizing, macros for layout generation) do not use HDL entry to capture design intent. However, HDL model development was used quite a bit for verification flows.

The fact that analog model development for speeding up analog physical design has no standard was also demonstrated at the Barcelona booth, where Navraj (and Stephen Boyd - CTO) extensively discussed their approach to building a mixed signal modeling language that is well suited for speeding up analog design.

Mazen showed the IP available from LTRIM and emphasized the importance of having verified and fully tested IP.

Juan Antonio pointed out the need to include content from actual analog IP companies. We discussed some of the mixed signal IP that IBM has on their web page (e.g., high speed I/O) and also that of Artisan. Since then, it is interesting that ARM is in the process of acquiring Artisan.

Steve Bibyk was part of the Semiconductor Research Corp. review of their Integrated Circuit and System Sciences (ICSS) contract work. The review was done at Ohio State in early September, the contracts were in the circuit design area, and involved about 24 university research projects, most of them in analog and mixed signal design. All the presentations showed examples of new analog circuits for a variety of applications: high speed serial I/O, data converters, PLLs, RF ESD structures, wireless analog front ends, etc. Almost all the contracts had test results and one theme that stood out was how inefficient it is to transfer a circuit idea into a design library element. The circuit ideas were either represented as models or schematics. The schematics would be standard if everyone used the same CAD tool, but the model descriptions weren't standardized even among users using the same CAD tools.

Since models (and their testbenches) are a rich category for standards development, here are some plans for the next content creation steps:

Information requests to the Analog Firm group:
Navraj - can you give the group some information on the modeling language approach you discussed at DAC?

Mazen - can you give an example of the type and format of macromodels used in LTRIM's products?

Juan Antonio – can you share the presentation (or some portion of it) in the Automated Macromodeling Techniques for Complex Mixed Signal Systems Tutorial?

Henry – can you give an example of models built in HDL that have close links to schematics and layout?

All - models that are part of physical design kits and layout generators?

Navraj noted that Barcelona is opening up their development on the MUSE modeling language which is targeted for analog design descriptions that would be synthesized using their optimization engines. Basically, the designer is now guided in writing macromodels that can be automatically converted to the posynomial forms used in the Barcelona optimization engines. The MUSE language appears to be a combination of SPICE and HDL constructs that enables the capturing of simulation testbenches in a language form, as opposed to the menu driven forms used in the Neolinear/Cadence tools. The use of modeling languages for analog synthesis could enable the design methodology to be offered by several vendor sources, as opposed to being locked into a single vendor.

Design Language for RF and Mixed Signal Synthesis.

Discussions with Barcelona indicate that the MUSE language will be initially targeted for Mixed Signal Design and Synthesis as opposed to RF synthesis. Their posynomial approach to building analog models and solving for the sizing parameters is more applicable to macromodeling methods where the designer builds the model from scratch, as opposed to using BSIM or similar detailed transistor models that are supplied from a foundry Physical Design Kit (PDK). Thus, the synthesis approach is more matched to high performance digital design, where large signal analog design modules and methods are used to achieve Gigahertz clocking and timing closure while reducing power consumption.

The Virtual Socket Interface (VSI) Alliance has launched a monthly newsletter and is soliciting Expert Viewpoint articles. Members of the Analog Firm group discussed the structure of the content for such an article on Analog Firm and Mixed Signal synthesis.

There was a one-on-one discussion with members of the VSIA Analog Firm group with regards to how Design Languages such as HDL can be correlated with the discoveries enabled by Analog and RF synthesis researchers. In particular, the use of Design Languages would be for library development, design re-use, and IP commercialization.

The following summarizes the trends of the discussion:
This program will develop a library of mixed signal and RF circuits being designed into a Cadence design framework, along with testbenches that contain performance calculations that can be compared to desired specifications. The design methodology will follow that of an automated analog synthesis approach. Mixed signal design environments that use HDLs will be linked with the design flows that are used for analog synthesis. Translation software and scripts will be developed to allow analog synthesis flows to use input structures that are specified in HDL formats. The main focus will be on analog testbench and model standardization and use of commercial CAD tools.

The research will use Virtuoso NeoCell and Virtuoso NeoCircuit in Cadence as well as the MUSE system by Barcelona Design. One of the challenges with using a NeoCircuit approach is that it is geared toward cell design and not system design. Neocircuit requires a designer to

translate system requirements into individual cell specifications, which are then used to drive the NeoCircuit sizing process. The mapping of system requirements into individual cell specifications is an optimization process performed by system designers as part of system decomposition.

The MUSE synthesis language is combined with a Geometric Programming (GP) simulator and enables a faster solution to systems with hundreds of thousands of unknowns. However, the designer is required to construct and calibrate all circuit models. Since hierarchical model building is what enables the process of translating system requirements to cell requirements, an objective of this research is to build the system models and testbenches needed for synthesis. Therefore, the strength of the Barcelona Design tools will be exercised at the system level to generate requirements that will be used by the NeoCircuit tools as individual cell specifications. The NeoCircuit tools also allow for the inclusion of process corners and other yield for design issues which can then be back annotated into the system level descriptions in MUSE, HDLs, or higher level languages.

The models used in the GP simulations will be calibrated against the more accurate models used in the Cadence simulators, so the basis of comparison will be the Cadence synthesis flow. Another reason to use the Cadence synthesis flow as the base methodology is the established linkage between schematics and layout generators, which is not available to us in the Barcelona Design flow.

Several key insights have been revitalized from the last 5 years of focused research into analog synthesis. One of them is that analog synthesis should be simulation based, using a systematic and heuristic approach to explore the design space via simulations. A second is that the test benches used for simulations need a high level of sophistication, incorporating design content that calculates performance metrics and compare these metrics to desired performance goals. Third, circuit and symbol design needs to be layout aware and, in fact, should be coupled to layout generators (or hierarchical parameterized cell generators – pcells).

Unfortunately, none of these three insights seem sufficiently recognized within the mixed signal HDLs (hardware description language) development community. Therefore, HDL methodologies for mixed signal design are widely different among users and are often used only as a method to speed up simulations via macro-modeling techniques.[1] Mixed signal system design continues to be an "art form" practiced by expert designers, who synthesize designs by hand. It is difficult to capture the experts' design intent, making re-use of the design by other, less experienced designers, a very time consuming endeavor. This situation increases analog design time and creates obstacles to meeting schedule and making market windows.

Thus, it is not surprising that effective analog synthesis methods are desired by various design groups and CAD vendors offer tools to address this need. Cadence has incorporated the Neolinear tools as part of their specification driven design flow. Other vendors offer alternate analog synthesis options. However, automating analog synthesis at the system level, such as for high speed serial I/O designs, still has a number of unsolved problems, such as hierarchical synthesis methods. In addition, the lack of standards in the area of analog synthesis and analog IP leads to difficulties in developing broad consensus on best practice methodologies for analog synthesis among SRC members and the larger IC design community.

Our research group has experience in both mixed signal HDL, plus digital and analog synthesis tools. Many system designs are moving toward increasing the digital content to enable both compensation and calibration of RF and analog baseband non-idealities in the analog modules. In addition, the digital circuit infrastructure used to compensate analog modules can often be used to make them reconfigurable, allowing for a more flexible and sustainable system design. The latter is especially important for military electronic systems that tend to have much longer legacy deployments than commercial electronics.

The digital infrastructure will be further developed using HDL constructs that facilitate use of well established digital synthesis methodologies. A compelling reason to develop an HDL based approach for high speed serial I/O designs is the ability to use HDL for the digital synthesis

[1] D. Fitzpatrick and I. Miller, Analog behavioral modeling with the Verilog-A Language, Kluwer Academic Publishers, 1998.

portion of mixed signal architectures. The analog portions of high speed serial I/O are embedded in a digital framework, since ultimately, digital symbols are sent across the communication channel. Another compelling reason to use an HDL based methodology is the ability to automatically generate design documentation in text or HTML based formats. The design documents can be generated in a manner that uses interoperability among CAD tools, as opposed to design content constrained to a particular proprietary format.

Standard HDL description methods will be developed for both analog component models and the associated performance-linked testbenches that are used by the analog synthesis tools. These standard description methods will be linked as close as possible to Verilog-AMS and VHDL-AMS design constructs, as well as high level Electronic System Languages such as SystemVerilog and SystemC.

Two CAD tool systems were evaluated for Analog Re-use. One was by SystemVision from Mentor Graphics. There is a student version of this tool that can be downloaded for free, although the OSU research program is also using the professional version. The CAD tool was evaluated for a PLL design, such as used as a frequency source for RF systems. The main advantage of SystemVision is the schematic entry tool well interfaced with a design language for synthesis. In this case, Mentor is pushing the use of VHDL-AMS, but other design languages are being supported also. The CAD tool is being evaluated as a design database manager of designs that are done in the Cadence tools, such as the former Neolinear tools being used for RF/analog synthesis.

The other CAD tool was the STAR-SPICE system developed at Stanford as part of the DARPA Marco center for Circuits and System Solutions (C2S2). STAR stands for Schematic Tool for Analog Reuse and enables a circuit designer to add executable comments to a schematic. The comments capture circuit performance goals and requirements constraints, similar to the information that is input to NeoCircuit.

RF/Analog IP Conclusions

Probably the key result from RF/Analog synthesis research is that the effective strategy is to accelerate what an experienced designer needs to get done, which then turns out to also be the main requirement for design re-use and RF/Analog IP. In simplistic terms, an experienced designer runs many different types of simulations to make design decisions at the schematic level. A simple term for these decisions is sizing. Once all the sizing decisions are done, IC layout is the next step. Since IC layout is tedious, time consuming, and needs major rework if any sizing decisions need to change, speeding up IC layout is also a key requirement for synthesis and re-use. One effective method to speed up IC layout is to use parameterized cells (p-cells) in a place and route tool. The combination of p-cells with place and route will be referred to as layout generators. Finally, after layout is accomplished, the schematics need to be updated to include the layout parasitics. The Neolinear tools were one of the most effective CAD packages to encompass the above acceleration of the RF/Analog design flow.

Unfortunately, there is no standard language or set of constructs to describe the above acceleration methods. One would hope that since simulations are model driven approaches, that standard modeling languages such as HDL-AMS (Hardware Description Language-Analog and Mixed Signal) would be used. However, this is not the case, since HDL-AMS does not standardize the simulation method, only the modeling method. Nevertheless, since HDLs are inherent in nearly all recent innovations in digital and software design flows (and many mixed signal systems such as Software Radar will use large digital cores and software to achieve new performance), HDL-AMS will eventually need to be fixed for RF/Analog re-use and synthesis.

The Analog Firm group in the VSIA worked on the development to standardize the methods for RF/Analog IP. Two of the main methods were to use the MUSE language from Barcelona-Design, which was being released for public use. The other method was to use the HDL-AMS development from Mentor Graphics, since HDL-AMS was also an IEEE standard. Unfortunately, both methods ran into roadblocks. Barcelona Design has folded as a company and the MUSE language is no longer available. The HDL-AMS approach at Mentor Graphics is not being positioned for RF/Analog synthesis at this time. At present, the only remaining language

and set of constructs for RF/Analog re-use is the proprietary constructs that are part of the Neolinear CAD tools.

There are several concerns when relying on proprietary constructs for re-use. First, in many design groups, designers use tools from a variety of CAD vendors. In many cases, a specific task is accomplished in a point tool and, in general, the complete set of tools from a given vendor is not the best set of point tools. For example, the behavioral modeling of RF modules in ADS is more effective for the designer than using Verilog-AMS for RF modules in Cadence, since the ADS tool has an efficient method to curve fit to determine the behavioral module parameters. RF testbenches are often more effective in ADS than in SpectreRF. Thus, there is a need to move and synchronize design content among different vendor's tools. In some cases, this is made easier by vendor cooperative agreements, such as those between Cadence IC tools and Agilent ADS. However, these agreements are often fragile, as both vendors position revise their tools to replace the functionality of the partner. Second, the typical user has a difficult time knowing exactly what content needs to be transferred between tools. For example, in a simulation environment, there are many implicit constructs that are entered into the CAD tool that are buried in the CAD tool database and thus difficult to track and archive. Many CAD vendors do this since it locks the user into purchasing future upgrades of their tools. One of the reasons that RF/Analog IP has been difficult to develop is due to the fact that many of the implicit CAD tool database constructs are hidden or implicit to the user, so that if a user wanted to become an IP provider and another user wanted to be an IP integrator, both the provider and the integrator do not have an explicit, negotiable list of design content that they can exchange between themselves. Usually, both the provider and integrator need to be using the same CAD tool database and a complete data exchange is required, essentially removing the possibility of the provider from retaining intellectual property. Thus, in many cases, the provider supplies a very limited re-use aspect of the design module, such as a layout and behavioral model.

RF/Analog IP re-use seems to have a more viable path when done within the same organization. In this case, the loss of intellectual property by the provider may not have the same level of concern. The final task of our research program was to provide some methods and software for internal re-use. The software would be used to automate the production of design capability

content, by capturing in one sheet the key demonstration of a working IC module. The sheets would contain object views of design content such as schematics, simulation plots, layouts, and descriptions of the object views. A UNIX/latex script file would organize the sheets into presentation format for IC integrators.

C. AFRL Design Center and NeoCAD tools

This section of the report summarizes the work done by Steve Bibyk and his students at the AFRL design center and at the various NeoCAD related meetings and review sessions. A number of design documents were developed and exchanged with the AFRL design center and NeoCAD community. There is also a review of exercising some of the NeoCAD tools, such as the Freeda simulation environment. The work program is described in approximately chronological order

We researched designs involving transformer feedback as a test vehicle to exercise upcoming NeoCAD tools. LNAs and mixers with transformer feedback will need simultaneous EM and circuit solvers in the design flow.

We downloaded the Freeda simulator being developed as part of the NeoCAD program. Initial installation needs to be on Linux machines at this time.

We attended the Freeda workshop organized by Michael Steer at NCSU. Overall, the workshop was effective in presenting cutting edge circuit simulation research. Still need to determine how Freeda will fit into design flows for future chip tape outs. Summarized view of how Freeda can fit into future design flows in a set of emails with Michael Steer. Continued review of Freeda source code and documentation for circuit design analysis with the BSIM4 model. Freeda looks most useful for those designers who need to develop their own models, rather than being handed a black box model from some fab process characterization. Analyzed the use of the Electric CAD system as a framework for Freeda. Experimented with the Freeda EM simulation environment, including the EM tools from UIUC.

Replied to information requests on the Freeda workshop from Charles Linding and Mark Kellum at Booz Allen Hamilton and J. Rockway at Spawar.

Developing CAD tool link between the Mentor Graphics System level modeling tools with the Cadence/ADS tool combination for system level modeling of RF system on a chip design.

Sent an S Band LNA-Mixer design report to Prof. Ranga Vemuri at UC as an application for his parasitic aware layout synthesis CAD tools. Sent the S Band LNA-Mixer design report to Thoma Vu at Top-Vu technology as technical background for the AFRL radar receiver on a chip development.

Attended the NeoCAD review in Washington DC. Analyzed CAD tools from NeoCAD for insertion into design flows.

Reviewed presentations from the March 6 Preliminary Design Review for Receiver on a Chip Demonstration.

Analyzed possible use of University of Cincinnati synthesis tool for analog design in future tape outs.

Met with Dr. Mantooth's student about use of their tools in design center tape out flow and discussed CMOS LNA design styles with Aji Mattamana. Participated in the Neolinear tool set up in design center.

Presented at the PDR for the upcoming FDSOI run. Interacted with the Boeing engineers at the design center. They asked for a copy of Dave Bayer's MS thesis and it was sent.

Attended the NeoCAD/Team meeting in Monterey. One main result from the first NeoCAD/Team meeting is that process technologies continue to improve at a very rapid rate, enabling RFIC design to extend well beyond X band, toward W band.

The CAD tools developed under NeoCAD cover many aspects of analog design. The CAD tools specific to RFIC design need to combine EM solvers with circuit solvers.

There is also the issue of building device models into the simulators that will work up to W band frequencies.

Trial Freeda and EM simulations. IC wave is the main tool. UIUC2D is for very limited structures. The Freeda simulation environment includes the UIUC2D and Prime simulation tools from UIUC. All three tools have problems and are not very helpful in IC design for tape out. A major selling point of Freeda is the ability to add EM models of various components, such as interconnects and coupled inductors. The tools from UIUC were supposed to enable the addition of EM effects into Freeda. However, UIUC2D is only for modeling infinitely long transmission lines and is of little utility. Prime builds spice netlists for use in Freeda, but Freeda has usage problems of its own. One of the main concerns is that this is university developed software and thus needs considerable work to enable the software to be used in a design to tape out activity. At the NeoCAD meeting, it was announced that there is another EM tool being developed out of UIUC known as ICwave for 3D EM analysis. This would be much more useful than UIUC2D, but we haven't seen any of this new software.

Tried some of the initial example files provided with Freeda. There are problems with them and it is unclear whether it is worth the effort to get them solved.

Freeda /apps/Freeda/current/test/ac.net ac.out

********** fREEDA 1.0 running on Tue Sep 9 13:56:35 2003 **********
*** Parsing input netlist ...

vccs:g1 1 2 0 0 g=1e-3 ri=1e3 ro=2e3
^
Parse Error near line 7
Element type vccs does not exist.

There are three AC analysis test circuits provided with Freeda. Only one of them works correctly.

ac.net crashes on initial parsing b/c of the vccs element. The file .../simulator/Freeda.cc seems to manage the main processes and calls yyparser to handle parsing netlists. The .../simultor/inout/parser.h header declares yyparse, but there is no parser.cc file. There is a parser_functions.cc file (which seems to match some other parser.h function), but it does not have yyparse in it. I am not enough of a C hack to know, but I am guessing/hoping yyparse must be some std c-function... I think that we somehow end up in the .../simulator/network/Circuit.cc code, which calls .../simulator/network/ElementManager.cc's createElement:

The testbench .../test/unityp.net also crashes, but upon Initializing Elements. The main Freeda.cc calls init() to initialize elements and apparently reaches a system level failure before returning and dies with "Abort" as the only message. The init() function is in the .../simulator/inout/init_clean.cc file and is fairly well error controlled. Mostly variables are set and i/o files opened (with error trapping). My best guess is that the initScan code is crashing:

```
void InitScan(FILE *f)
{
 yyin = f;
 thisSymT_P = NULL;
 maimed = FALSE;
 polydimension = 0; /* zero initial polynomial dimension */
}
```

there is one AC analysis that completes correctly for me:
.../test/tline1.net
The actual AC analysis is seemingly managed from the

.../simulator/analysis/AC.cc code, however the heart of the code seems to be generating the MNAM matrix in the .../simulator/analysis/FreqMNAM.cc code. Each MNAM vector is created:

Participated in the 10/15/03 meeting at the design center with Anantha Krishnan from Darpa and the Neolinear NeoCAD team.

Participated in the 11/5/03 DARPA brainstorming session at Booz, Allen, & Hamilton to develop content for a proposal to achieve an extension to the NeoCAD program.

Neolinear Demonstration of CAD tool use (via WebX) showed some noteworthy design issues in RFIC design. Part of the demo example was an LNA centered at 1.5 GHz. Moving one of the layout inductors showed a dramatic change in S11, even though the design geometries were at 1/100 of a wavelength. This demonstrated that for RFIC design, the metal layers are so thin that loss effects dominate, and models of lossless transmission lines (Z= ~L/C) are not appropriate. This is quite different from discrete RF design.

At the DARPA brainstorming session, Steve Bibyk outlined a desired mixed signal design flow from specification development to physical design. R. Singh noted that a similar design flow had been advocated by Ken Kundert at Cadence, known as the “Dune” project, but was never made public. Need to find out how far Cadence took the Dune project.

Also, R. Singh talked about the difference between hard, firm, and soft IP (Intellectual Property) for silicon chip design. These definitions were somewhat confusing to the brainstorming group. Bibyk reviewed some of the Orora design tools with Len Orlando at the design center. In particular, they discussed the Arsyn synthesis tools.

Bibyk also reviewed the slides that Charles Cerny was planning to present at the DARPA/FCRP review being held at MIT.

Bibyk sent out the most recent Analog Firm document to the VSIA group and then met with that group at the 2004 Design Automation Conference. The Analog firm document was also sent to Anthony Gadient of Cadence and to Warren Snapp of Boeing. Some summary items are:
1. VSIA leadership of the Analog Firm group is now done by Juan Antonio Carballo, a mixed signal system architect at IBM, Austin, TX. VSIA has also reorganized to be more responsive to

its membership, setting up three main thrusts in IP Quality, IP Protection, and IP R&D. J. Carballo is the director of the IP R&D thrust. Steve Bibyk is still the integrator for the Analog Firm work.

2. The VSIA activity will be correlated with the OpenAccess Database effort developed by the Silicon Integration Initiative (www.si2.com). This group is made up of users and developers of CAD tools, with the goal that all the CAD tools should use the same database. This allows users to integrate their own tool flows and to allow straightforward comparisons of CAD tools on the same design. For example, in the NeoCAD program, Neolinear used the OpenAccess Database, but other programs did not.

III. Main Results

The key result from RF/Analog synthesis research is that the most effective strategy is to accelerate what an experienced designer needs to get done. Accelerating the activities of an experienced designer also turns out to be the main requirement for design re-use and RF/Analog IP. In simplistic terms, an experienced designer runs many different types of simulations to make design decisions at the schematic level. A simple term for these decisions is sizing. Once all the sizing decisions are done, IC layout is the next step. IC layout is tedious, time consuming, and needs major rework if any schematic sizing decisions need to change. Speeding up IC layout is also a key requirement for synthesis and re-use. One method that helps layout is to reduce the time needed for other tasks, such as having to resize schematics. Another effective method to speed up IC layout is to use parameterized cells (p-cells) in a place and route tool. The combination of p-cells with place and route will be referred to as layout generators. Finally, after layout is accomplished, the schematics need to be updated to include the layout parasitics. The Neolinear tools were one of the most effective CAD packages to encompass the above acceleration of the RF/Analog design flow.

Unfortunately, there is no standard language or set of constructs to describe the above acceleration methods. One would hope that since simulations are model driven approaches, that standard modeling languages such as HDL-AMS (Hardware Description Language-Analog and Mixed Signal) would be used. However, this is not the case, since HDL-AMS does not standardize the simulation method, only the modeling method. Nevertheless, since HDLs are

inherent in nearly all recent innovations in digital and software design flows (and many mixed signal systems, such as Software Radar, will use large digital cores and software to achieve new performance), HDL-AMS will eventually need to be fixed for RF/Analog re-use and synthesis.

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There are several concerns when relying on proprietary constructs for re-use. First, in many design groups, designers use tools from a variety of CAD vendors. In many cases, a specific task is accomplished in a point tool and, in general, the complete set of tools from a given vendor is not the best set of point tools. For example, the behavioral modeling of RF modules in ADS is more effective for the designer than using Verilog-AMS for RF modules in Cadence, since the ADS tool has an efficient method to curve fit to determine the behavioral module parameters. RF testbenches are often more effective in ADS than in Cadence SpectreRF. Thus, there is a need to move and synchronize design content among different vendor's tools. In some cases, this is made easier by vendor cooperative agreements, such as those between Cadence IC tools and Agilent ADS. However, these agreements are often fragile, as both vendors position their tools to replace the functionality of the partner. Second, the typical user has a difficult time knowing exactly what content needs to be transferred between tools. For example, in a simulation environment, there are many implicit constructs that are entered into the CAD tool that are buried in the CAD tool database and thus difficult to track and archive. Many CAD vendors do this since it locks the user into purchasing future upgrades of their tools. One of the reasons that RF/Analog IP has been difficult to develop is due to the fact that many of the implicit CAD tool database constructs are hidden or implicit to the user, so that if a user wanted to become an IP provider and another

user wanted to be an IP integrator, both the provider and the integrator do not have an explicit, negotiable list of design content that they can exchange between themselves. Usually, both the provider and integrator need to be using the same CAD tool database and a complete data exchange is required, essentially removing the possibility of the provider from retaining intellectual property. Thus, in many cases, the provider supplies a very limited re-use aspect of the design module, such as a layout and behavioral model.

RF/Analog IP re-use seems to have a more viable path when done within the same organization. In this case, the loss of intellectual property by the provider may not have the same level of concern. The final task of our research program was to provide some methods and software for internal re-use. The software would be used to automate the production of design capability content, by capturing in one sheet the key demonstration of a working IC module. The sheets would contain object views of design content such as schematics, simulation plots, layouts, and descriptions of the object views. A UNIX/latex script file would organize the sheets into presentation format for the designers who are IC integrators.

RF and analog design are accomplished by using simulations to make design decisions. Thus, re-use of a design means being able to re-run simulations to change the design decisions, or sizing. The new sizes are then propagated to layout generators for rapid tape out. These layout generators are evolutions of pcells, along with place are route optimizers.

Running simulations means that for larger designs, macromodels will need to be used. One of the main advantages of ADS for RF design is the simulation and built in macromodel capability of this CAD tool.

IV. Conclusions and Recommendations

Several LNA modules were designed to completion and fabricated to obtain insight into all the constructs needed for RF/Analog re-use. Although there were testing difficulties with the LNAs, the design activity did discover many of the activities and design content needed for an LNA design module. Another reason for performing the LNA design was to do the initial design work

for reconfigurable RF modules. Future system designs such as Software Radars are expected to have RF modules that are reconfigured by the digital processing core for higher performance. For example, our LNA was fabricated in the MIT LL SOI process, which was part of a radar system design that used proprietary digital signal processing to enhance dynamic range, such as nonlinear compensation for enhancing Spurious Free Dynamic Range (SFDR). Nevertheless, the requirements for the RF and digital processing modules were such that the modules could be designed separate from each other and brought together at the final integration step. However, a method to achieve additional dynamic range would be to make the LNA adaptable, such that its operation depended on the strength of the received radar signal. For very weak signals, the LNA could be adapted to improve noise figure, whereas for stronger signals, the LNA could be adapted for improved linearity. The adaptation would be controlled by the digital core to enable signal processing to determine the adaptation process. One of the main difficulties with adaptable or reconfigurable RF/Analog designs is the need to couple the modules so that they can not be designed separately from each other.

The main benefit of doing the LNA was to understand all aspects of the RF design process for re-use related synthesis. David Bayer's Chp. 2 on Design Re-use methodologies conveys useful design flow content. Verilog A didn't work well for re-use; it is better in ADS. The RFDE software enabled Neolinear to do RF synthesis.

VSIA Extension Specification.

Barcelona Design disappeared. Mar and Navraj left, and Singh moved on. The hypothesis was that Analog and RF reuse could be specified independent of CAD tools, and so could synthesis, which is the new element to analog IP. However, at this time, analog synthesis, and its utilization for analog IP, is CAD vendor specific, with the Cadence tools being the leading vendor for the AFRL design center.

In an RF/Analog design flow, much of the design content in captured in the CAD tools database. The design content is not evident in the design documentation. In many cases, multiple CAD tools need to be integrated together. For example, Cadence, ADS, digital tools in either Synopsis or Mentor Graphics, and Microwave Office. Since each CAD tool uses a different database and

scripting methodology, there are problems in using the tools. Much of a design is specific to a CAD tool vendor.

System development will still need to use some combination of HDLs and behavioral macromodeling. Macromodeling in Cadence was inefficient. Not only do circuits need to be macromodelled, but so do performance calculations. This is known as Results extraction from the simulation waveforms. In Cadence, this is often accomplished using the calculator function after running a simulation. Another possibility is to use the ocean scripting language. ADS built in these types of operations so that they can be placed on a schematic for a simulation and thus be part of an optimization routine for synthesis.